Data Book
OEMmodule 486™

Full-Featured 100MHz
486SX PC *OEMmodule™*

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General Description

OEMmodules combine system hardware, software, and solid state mass storage in a single compact device.

The OEMmodule 486 is a PC/AT-compatible 80486SX motherboard and standard peripheral interfaces in a 240-pin surface-mount integrated circuit module.

The OEMmodule 486 includes all standard PC/AT motherboard functions, 2M bytes of internal DRAM, 2M bytes of internal flash, serial and parallel I/O, floppy and IDE disk controllers, ISA expansion bus, and a standard AT BIOS.

The unique chip-like design of the OEMmodule 486 makes it ideally suited for products where low power consumption, high reliability, and minimal size are essential. The module requires a minimum number of external components, making it ideal for embedded systems.

The OEMmodule 486's compatibility with the PC/AT ISA (Industry Standard Architecture) bus and PC/104 bus allows you to easily integrate a wide selection of low-cost PC peripherals, as well as your own proprietary hardware designs. Standard serial ports, parallel port, floppy, and hard disk interfaces allow you to use standard peripherals and cables in your design.

You can develop your own application software on a desktop PC/AT and transfer your code directly to the embedded system with little or no modification. The module's standard BIOS and DOS (or other operating system on disk) let you develop your application software using standard operating systems, drivers, software libraries, and software development tools. You can easily field-upgrade the BIOS, DOS operating system, CMOS configuration parameters, and installed application programs over a serial port using the module's innovative Download Interface.

Features

486SX 100 Mhz CPU

- Full 32-bit internal architecture; cost-effective 16-bit external bus
- Up to 64M bytes physical memory
- Virtual memory, paging, and hardware-enforced protection

PC Core Logic

- AT-compatible DMA controllers, interrupt controllers, timer/counters
- Standard AT keyboard controller and real-time clock

PC BIOS

- Standard AT BIOS functionality
- Support for OEM BIOS customization
- Setup information stored in non-volatile Flash EPROM, allowing battery-free operation

Serial Ports

- Two independent 16550-compatible serial ports
- LSTTL signal levels (single-chip conversion to RS232C)
- Baud rates up to 115K Baud

Bi-Directional Parallel Port

- Standard Mode: IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bi-directional Parallel Port
- Enhanced Mode: Enhanced Parallel Port (EPP) compatible
- Up to 24 mA drive current

DRAM

- High performance muxed DRAM interleave, CPU pipelined operation
- 2M bytes internal DRAM
- Compatible with standard PC SIMMs and page-mode DRAMs (70 nS)
- Shadowed BIOS

Floppy Disk Controller

- Supports all standard PC floppy formats
- Software compatible with 765B controller and PC BIOS
- Integrated digital data separator for high reliability and noise immunity
- Supports up to two floppy drives

EIDE Hard Drive Interface

- Full 40-pin interface to IDE or EIDE hard disk drive
- Supports up to two drives (master/slave)
- LED activity light support

Solid State Flash Memory Device

- 1.4Mb (formatted) Resident Flash Disk for OEM software
- Expandable by adding external Flash memory devices

ISA Bus

- Subset of standard PC/AT expansion bus
- Supports PC/104 implementation

Power Monitor

- Brownout protection
- Resistor-settable voltage threshold
- Provides a reliable reset signal if power fluctuates

Electrical Specifications

- 5 volt only operation
- Requires +5VDC ±5% @ 600mA
- Typical system with 2M DRAM: 550 mA at 100Mhz operation

Dedicated Power Management Unit

- Extends Battery Life
- Suspend and Standby Power Settings
- Selectable Activity and Wakeup Events
- Software Controllable

Mechanical/Environmental

- Package: 2.20 x 3.00 x .450 inches (56 x 76x 11 mm)
- 240 (50 x 70) .014 Gull-wing pins on .040 centers (1.016 mm pitch), surface mount
- Standard Operating temperature: +32F to +158F (0C to +70C)
- Storage temperature: -40F to +212F (-40C to +100C)
- Weight: 5 oz (140 gm)
- Package pin order is optimized for efficient layout routing

Off-module Requirements

- DRAM (optional — needed only if you require more than 2 Mbytes of DRAM.) — up to 64M bytes of EDO or fast-page. Use 3.3 Volt 30-pin SIMMs, 72-pin SIMMs, ISO DIMMs (single sided), or discrete memory chips)
- Various pull-up and pull-down resistors (described in this document)
- RS232C or RS485 voltage interface components for serial ports (optional)
- 3.6 V lithium cell for RTC backup (optional)

Contents

ORDERING INFORMATION

MOD-486-Q-01—486SX 100MHz with 2MB DRAM, 2MB built-in flash, 2 serial & 1 parallel port, floppy and EIDE controllers, and BIOS. Does not include manuals or utility disk.

SCX-486-K-01 (ZF SystemCard™ Developm Kit)— 5.23" form factor with OEMmodule 4986-100MHz, 18MB DRAM, 2MB built-in flash, SVGA controller, 10BaseT Ethernet, speaker, BIOS, technical manuals, cables and utility software.

104-486-K-01 (ZF 104Card™ 486 Development Kit)—PC/104 module with OEMmodule 486-100MHz, 2MB DRAM,2MB built-in flash, 2MB additional onboard flash (4MB total), 4 serial and 2 parallel ports, BIOS, technical manuals, cables and utility disk.

SLC-486-K-01 (ZF SlotCard™ 486 Development Kit)— AT-ISA bus card form factor with OEMmodule 486-100MHz, 2MB DRAM, 2MB built-in flash, SVGA controller, speaker, BIOS, technical manuals, cables and utility software. Does not include external DRAM or flash.

Technical manuals and utilities are available on the ZF Microsystems CD.

Specifications

Absolute Maximum Ratings*

Absolute Maximum Voltage on any pin, with respect to Ground ..... -0.3V to +6.5V

Storage Temperature (case) .....-40°C to +100°C (-40°F to +212°F)

Lead Temperature (soldering, 10 seconds) .....+325°C (+617°F)

Operating Conditions

Supply Voltage (VCC) .....+4.75V to +5.25V

Case Temperature (under bias) .....0°C to +70°C (+32°F to +158°F)

* Stresses above those listed above can cause permanent damage to the device. These values are stress ratings only, and do not imply that the device should be operated at these extremes. Voltage and temperature exposure beyond the *Operating Conditions* may affect device reliability.

Some DC power supplies exhibit voltage spikes when AC power is switched on or off, or during AC power line voltage transients. Use DC power supply clamp circuits to prevent damage to the module.

DC Electrical Characteristics (TA = 0°C to +70°C, VCC = +5.0V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Voltage Input Low	V_{IL}			0.8	V	*
Voltage Input High	V_{IH}	2.0			V	*
Input Current	I_{IL}	-10	1	+10	µA	*
Battery Current	I_{BATT}		4.8	10	µA	
Some inputs have pull-ups. See the ISA Expansion Bus connector tables for specifics.						

Table 1. Input Current

Voltage Output		Min	Max	Current
DRAM Memory				
MA[00:11]	V_{OH} V_{OL}	2.85	 0.45	12 mA 12 mA
RAS[0:3],DRWE	V_{OH} V_{OL}	2.85	 0.45	12 mA 12 mA
MD[0:15], DP[0:1]	V_{OH} V_{OL}	2.85	 0.45	12 mA 12 mA
CAS[H/L][0:3]	V_{OH} V_{OL}	2.85	 0.45	18 mA 18 mA

ISA Bus				
SA[0:19]	V_{OH} V_{OL}	2.85	 0.45	12 mA 12 mA
SD[0:15]	V_{OH} V_{OL}	2.85	 0.45	12 mA 12 mA
IOW, IOR, MEMR	V_{OH} V_{OL}	2.85	 0.45	12 mA 12 mA
MEMW	V_{OH} V_{OL}	2.85	 0.45	12 mA 12 mA
DACK[1:2]	V_{OH} V_{OL}	2.85	 0.45	12 mA 12 mA
RESETDRV	V_{OH} V_{OL}	2.85	 0.45	3 mA 3 mA
BALE, AEN, SBHE	V_{OH} V_{OL}	2.85	 0.45	12 mA 12 mA
IDE Interface				
HDIOR, HDALE	V_{OH} V_{OL}	2.4	 0.8	4 mA 12 mA
HA[0:2], HDCS	V_{OH} V_{OL}	2.4	 0.8	12 mA 24 mA

Table 2. Output Current (1)

Voltage Output		Min	Max	Current
Floppy Interface				
MTR[0:1]	V_{OH} V_{OL}	2.4	 0.8	48 mA (open drain) 48 mA (open drain)
DRV[0:1]	V_{OH} V_{OL}	2.4	 0.8	48 mA (open drain) 48 mA (open drain)
DIR, STEP, WDATA	V_{OH} V_{OL}	2.4	 0.8	48 mA (open drain) 48 mA (open drain)
WGATE, HDSEL	V_{OH} V_{OL}	2.4	 0.8	48 mA (open drain) 48 mA (open drain)

Miscellaneous				
PFO, MR, WDO	V_{OH} V_{OL}	2.6	 0.3	4 mA 4 mA
SPKR	V_{OH} V_{OL}	2.85	 0.45	4 mA 4 mA
RTCIRQ	V_{OH} V_{OL}	2.85	 0.45	4 mA 4 mA
KDATA, KCLOCK	V_{OH} V_{OL}	2.4	 0.8	4 mA 4 mA
Serial Ports				
TxD outputs	V_{OH} V_{OL}	2.4	 0.8	12 mA 24 mA
All Other Outputs	V_{OH} V_{OL}	2.4	 0.8	2 mA 4 mA
Parallel Port				
PD[0:7]	V_{OH} V_{OL}	2.4	 0.8	24 mA (open drain) 24 mA (open drain)
SLCTIN, INIT, AUTOFD	V_{OH} V_{OL}	2.4	 0.8	24 mA (open drain) 24 mA (open drain)
STRB	V_{OH} V_{OL}	2.4	 0.8	24 mA (open drain) 24 mA (open drain)

Table 2. Output Current (2)

Parameter	Symbol	Maximum	Unit
Input Capacitance	CIN	10	pF
Output Capacitance	COUT	20	pF

Table 2. Capacitance (TA = 25 °C, Vcc = +5.0V)

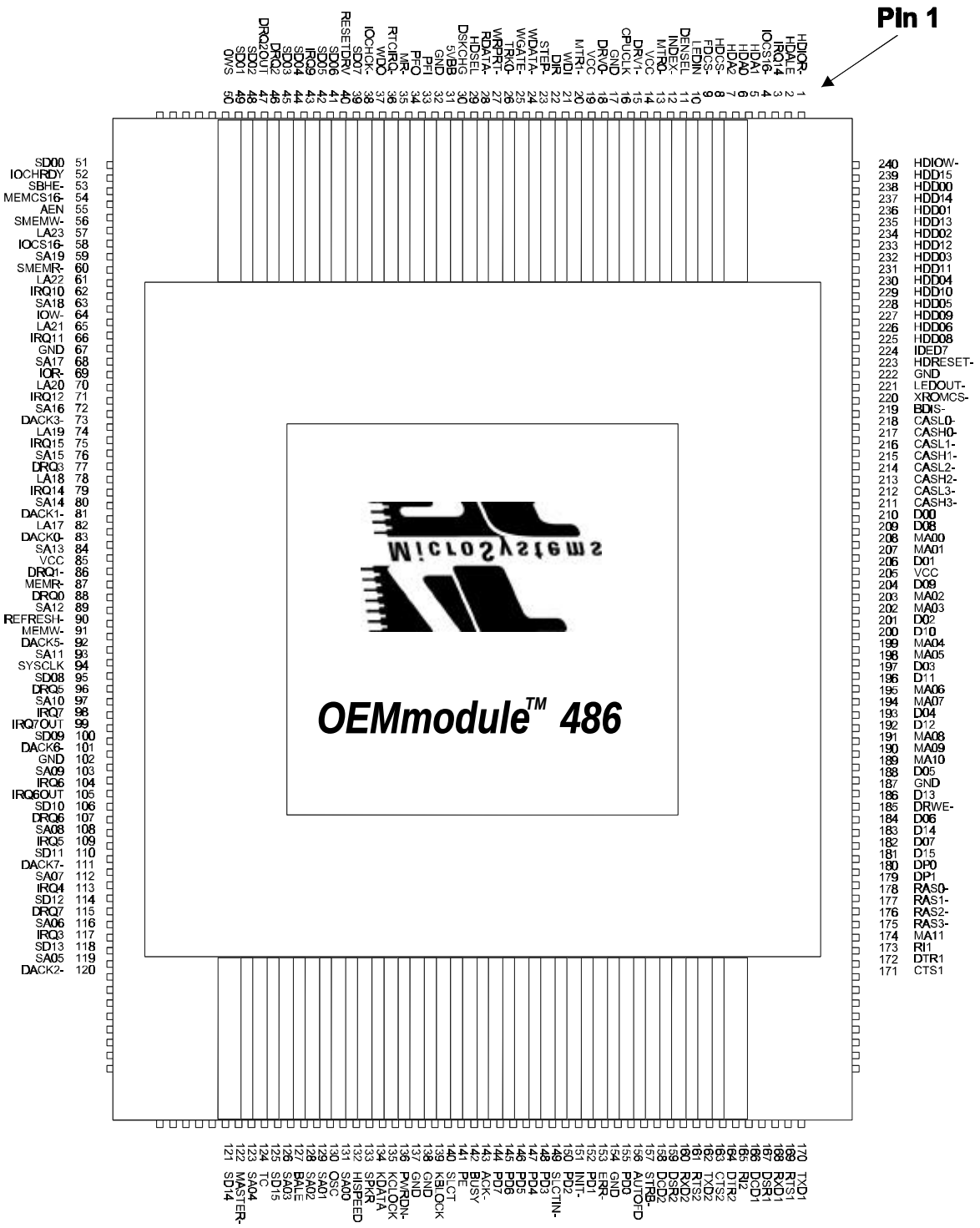


Figure 1. Pin Diagram

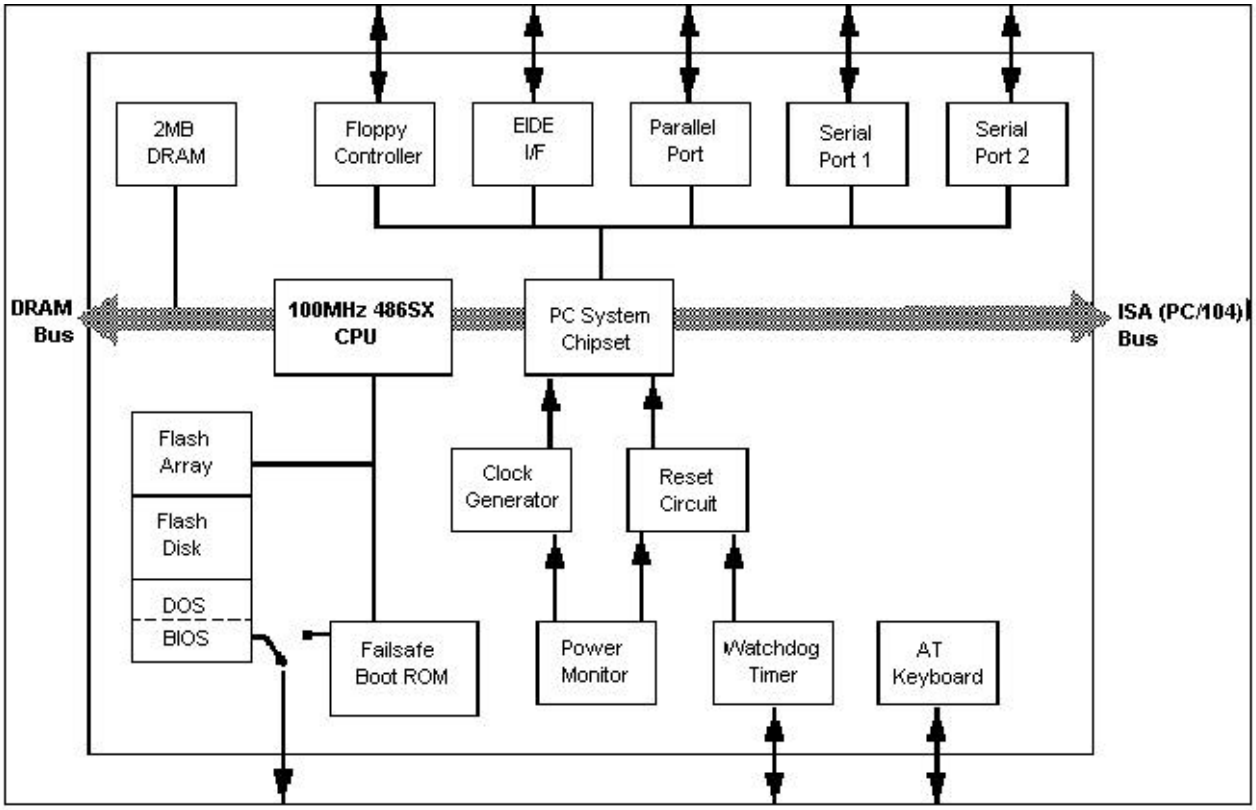


Figure 2. Internal Block Diagram

Alphabetic Pin List

Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin
0WS- (1)	50	D11	196	CPUCLK	16	HDD05	228	IRQ14	79
ACK-	143	D12	192	DRWE-	185	HDD06	226	IRQ15(1)	75
AEN	55	D13	186	DSKCHG	30	HDD08	225	IRQ3	117
AUTOFD	156	D14	183	DSR1	167	HDD09	227	IRQ4	113
BALE	127	D15	182	DSR2	159	HDD10	229	IRQ5	109
BDIS-	219	DACK0-(1)	83	DTR1	172	HDD11	231	IRQ6	104
BUSY	142	DACK1-	81	DTR2	164	HDD12	233	IRQ6OUT	105
CASH0-	217	DACK2-	120	ERR-	153	HDD13	235	IRQ7	98
CASH1-	215	DACK3-(1)	73	GND	17	HDD14	237	IRQ7OUT	99
CASH2-	213	DACK5-(1)	92		32	HDD15	239	IRQ9	43
CASH3-	211	DACK6-(1)	101		67	HDIOR-	1	KBLOCK	139
CASL0-	218	DACK7-(1)	111		102	HDIOW-	240	KCLOCK	135
CASL1-	216	DCD1	166		137	HDRESET	223	KDATA	134
CASL2-	214	DCD2	158		138	HDSEL	29	LA17	82
CASL3-	212	DENSEL	11		154	HISPEED	132	LA18	78
CTS1	171	DIR	22		187	IDED7	224	LA19	74
CTS2	163	DP0 (1)	180		222	INDEX-	12	LA20	70
D00	210	DP1 (1)	179	HDA0	6	INIT-	151	LA21	65
D01	206	DRQ0(1)	88	HDA1	5	IOCHCHK-	38	LA22	61
D02	201	DRQ1	86	HDA2	7	IOCHRDY	52	LA23	57
D03	197	DRQ2	46	HDALE	2	IOCS16-	4	LEDIN	10
D04	193	DRQ2OUT	47	HDCS0-	8		58	LEDOUT-	221
D05	188	DRQ3(1)	77	HDCS1-	9	IOR-	69	MA00	208
D06	184	DRQ5(1)	96	HDD00	238	IOW-	64	MA01	207
D07	182	DRQ6(1)	107	HDD01	236	IRQ10(1)	62	MA02	203
D08	209	DRQ7(1)	115	HDD02	234	IRQ11(1)	66	MA03	202
D09	204	DRV0-	18	HDD03	232	IRQ12(1)	71	MA04	199
D10	200	DRV1-	15	HDD04	230	HDIRQ	3	MA05	198

(1) These signals are not supported on the OEMmodule 486.

Table 3. Alphabetic Pin List (1 of 2)

Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin
MA06	195	PD6	145	SA00	131	SBHE-	53	SMEMW-	56
MA07	194	PD7	144	SA01	129	SD00	51	SPKR	133
MA08	191	PE	141	SA02	128	SD01	49	STEP-	23
MA09	190	PFI	33	SA03	126	SD02	48	STRB-	157
MA10	189	PFO	34	SA04	123	SD03	45	SYSCLK	94
MA11	174	PWRDN-	136	SA05	119	SD04	44	TC	124
MASTER- (1)	122	RAS0-	178	SA06	116	SD05	42	TRK0-	26
MEMCS16-	54	RAS1-	177	SA07	112	SD06	41	TXD1	170
MEMR-	87	RAS2-	176	SA08	108	SD07	39	TXD2	162
MEMW-	91	RAS3-	175	SA09	103	SD08	95	VBAT	31
MR-	35	RDATA-	28	SA10	97	SD09	100	VCC	14
MTR0-	13	REFRESH-	90	SA11	93	SD10	106		19
MTR1-	20	RESETDRV	40	SA12	89	SD11	110		85
OSC	130	RI1	173	SA13	84	SD12	114		205
PD0	155	RI2	165	SA14	80	SD13	118	WDATA-	24
PD1	152	RTCIRQ-	36	SA15	76	SD14	121	WDI	21
PD2	150	RTS1	169	SA16	72	SD15	125	WDO	37
PD3	148	RTS2	161	SA17	68	SLCT	140	WGATE-	25
PD4	147	RXD1	168	SA18	63	SLCTIN-	149	WRPRT-	27
PD5	146	RXD2	160	SA19	59	SMEMR-	60	XROMCS-	220

(1) These signals are not supported on the OEMmodule 486.

Table 3. Alphabetic Pin List (2 of 2)

Pin Descriptions

Pin	Pin Name	Description	Type
1	HDIOR-	IDE I/O Read, active low. Buffered version of IOR-.	Out
2	HDALE	IDE Address Latch Enable, active high. Buffered version of BALE.	Out
3	HDIRQ	IDE Interrupt Request. Tied to pin 79 IRQ14. For use with IDE interface.	In
4	IOCS16-	IDE I/O Chip Select 16. A low requests a 16-bit transfer on the SA bus. Same signal appears on Pin 58. This one is used for the IDE interface.	In
5	HDA1	IDE Address 1. Buffered version of SA1.	Out
6	HDA0	IDE Address 0. Buffered version of SA0.	Out
7	HDA2	IDE Address 2. Buffered version of SA2.	Out
8	HDCS0-	IDE Chip Select. A low indicates that data is being transferred to or from the IDE drive.	Out
9	HDCS1-	IDE Chip Select. A low indicates that data is being transferred to or from the IDE drive.	Out
10	LEDIN	LED signal from IDE drive.	In
11	DENSEL	Floppy density select or RPM.	Out
12	INDEX-	Floppy disk index pulse, input from drive.	In
13	MTR0-	Floppy disk active low open drain output selects motor driver 0. The motor enable bits are software controlled via the floppy's Digital Output Register (DOR).	OD
14	VCC		
15	DRV1-	Floppy disk active low open drain output that selects floppy drive 1.	OD
16	CPUCLK	33 MHz CPU clock frequency output	Out
17	GND		
18	DRV0-	Floppy disk active low open drain output that selects floppy drive 0.	OD
19	VCC		
20	MTR1-	Floppy disk active low open drain output selects motor driver 1. The motor enable bits are software controlled via the floppy's Digital Output Register (DOR).	OD
21	WDI	Watchdog Timer Tickle Input. May be used as a system input to the Watchdog Timer. Leave open to disable the Watchdog Timer.	In
Key: In = TTL Input; Out = Output; OD = Open Drain/Collector Output; IS = Input with hysteresis			

Table 4. Pin Descriptions (1)

Pin	Pin Name	Description	Type
22	DIR	Floppy disk open drain output that controls floppy read/write head movement direction. Low = step in.	OD
23	STEP-	Floppy disk open drain active low output provides the step pulse to move the floppy read/write head.	OD
24	WDATA-	Floppy disk active low open drain signal writes serial data to the selected floppy drive. This is a high open current drain output and is gated internally with WGATE-.	OD
25	WGATE-	Floppy disk active low open drain signal that enables the head to write onto the floppy disk.	OD
26	TRK0-	Floppy disk active low Schmidt input indicates that the head is on track 0 of the selected drive.	IS
27	WRPRT-	Floppy disk active low Schmidt input indicating that the disk is write-protected. Any WDATA- command is ignored.	IS
28	RDATA-	Floppy disk active low Schmidt input that reads raw data from the floppy disk.	IS
29	HDSEL	Floppy disk open drain output that selects the head on the selected drive. Low = side 0.	OD
30	DSKCHG	Floppy disk input signal indicating that the floppy door has been opened.	IS
31	VBAT	Real-time clock backup battery (3.6 volt Lithium cell).	Ana-log
32	GND		
33	PFI-	Powerfail input, monitors external voltage input; low generates a PFO-. PFI- threshold is 1.25 volts.	Ana-log
34	PFO-	Powerfail output, indicating power is below threshold.	Out
35	MR-	Master Reset input; low resets computer.	In
36	RTCIRQ-	Alarm output from the onboard real time clock or input to IRQ8.	OD/ In
37	WDO-	Watchdog timer output; goes low if watchdog timer times out.	Out
38	IOCHCHK-	ISA gated non-maskable interrupt input.	In
39	SD07	ISA System Data 07.	I/O
40	RESET-DRV	ISA active high system reset signal.	Out
41	SD06	ISA System Data 06.	I/O
Key: In = TTL Input; Out = Output; OD = Open Drain/Collector Output; IS = Input with hysteresis			

Table 4. Pin Descriptions (2)

Pin	Pin Name	Description	Type
42	SD05	ISA System Data 05.	I/O
43	IRQ9	ISA Interrupt Request 9.	In
44	SD04	ISA System Data 04.	I/O
45	SD03	ISA System Data 03.	I/O
46	DRQ2	ISA DMA 2 Request strobe.	In
47	DRQ2OUT	Floppy DMA Request. Normally connected to DRQ2.	Out
48	SD02	ISA System Data 02.	I/O
49	SD01	ISA System Data 01.	I/O
50	0WS-	Not Supported.	In
51	SD00	ISA System Data 00.	I/O
52	IOCHRDY	ISA I/O Channel Ready. A low adds wait states to the current ISA bus cycle.	In
53	SBHE-	ISA System Byte High Enable.	Out
54	MEMCS16-	ISA 16-bit Memory Chip Select request. Indicates that the current memory transaction is 16-bits.	In
55	AEN	ISA Address Enable.	Out
56	SMEMW-	ISA System Memory Write strobe.	Out
57	LA23	ISA Latched Address 23.	Out
58	IOCS16-	ISA 16-bit I/O Chip Select request. Indicates that the current I/O transaction is 16-bits. Same signal appears on Pin 4.	In
59	SA19	ISA System Address 19.	Out
60	SMEMR-	ISA System Memory Read strobe.	Out
61	LA22	ISA Latched Address 22.	Out
62	IRQ10	Not Supported.	In
63	SA18	ISA System Address 18.	Out
64	IOW-	ISA !/O Write strobe.	Out
65	LA21	ISA Latched Address 21.	Out
66	IRQ11	Not Supported.	In
67	GND		
68	SA17	ISA System Address 17.	Out
Key: In = TTL Input; Out = Output; OD = Open Drain/Collector Output; IS = Input with hysteresis			

Table 4. Pin Descriptions (3)

Pin	Pin Name	Description	Type
69	IOR-	ISA I/O Read strobe.	Out
70	LA20	ISA Latched Address 20.	Out
71	IRQ12	Not Supported.	In
72	SA16	ISA System Address 16.	Out
73	DACK3-	Not Supported.	Out
74	LA19	ISA Latched Address 19.	Out
75	IRQ15	Not Supported.	In
76	SA15	ISA System Address 15.	Out
77	DRQ3	Not Supported.	In
78	LA18	ISA Latched address 18.	Out
79	IRQ14	ISA Interrupt Request 14Tied to pin 3 (HDIRQ). Not available if hard drive is present.	In
80	SA14	ISA System Address 14.	Out
81	DACK1-	ISA DMA 1 Acknowledge strobe.	Out
82	LA17	ISA Latched Address 17.	Out
83	DACK0-	Not Supported.	Out
84	SA13	ISA System Address 13.	Out
85	VCC		
86	DRQ1	ISA DMA 1 Request.	In
87	MEMR-	ISA active low memory read strobe.	Out
88	DRQ0	Not Supported.	In
89	SA12	ISA System Address 12.	Out
90	REFRESH-	Not Supported.	Out
91	MEMW-	ISA active low memory write strobe.	Out
92	DACK5-	Not Supported.	Out
93	SA11	ISA System Address 11.	Out
94	SYSCLK	ISA System Clock.	Out
95	SD08	ISA System Data 08.	I/O
96	DRQ5	Not Supported.	In
97	SA10	ISA System Address 10	Out
Key: In = TTL Input; Out = Output; OD = Open Drain/Collector Output; IS = Input with hysteresis			

Table 4. Pin Descriptions (4)

Pin	Pin Name	Description	Type
98	IRQ7	ISA Interrupt Request 7.	In
99	IRQ7OUT	Parallel port interrupt request. Normally connects to IRQ7.	Out
100	SD09	ISA System Data 09.	I/O
101	DACK6-	Not Supported.	Out
102	GND		
103	SA09	ISA System Address 09.	Out
104	IRQ6	ISA Interrupt Request 6.	In
105	IRQ6OUT	Floppy disk interrupt request. Normally connects to IRQ6.	Out
106	SD10	ISA System Data 10.	I/O
107	DRQ6	Not Supported.	In
108	SA08	ISA System Address 08.	Out
109	IRQ5	ISA Interrupt Request 5.	In
110	SD11	ISA System Data 11.	I/O
111	DACK7-	Not Supported.	Out
112	SA07	ISA System Address 07.	Out
113	IRQ4	ISA Interrupt Request 4, assigned to COM1, sharable	In
114	SD12	ISA System Data 12.	I/O
115	DRQ7	Not Supported.	In
116	SA06	ISA System Address 06.	Out
117	IRQ3	ISA Interrupt Request 3, assigned to COM2, sharable	In
118	SD13	ISA System Data 13.	I/O
119	SA05	ISA System Address 05.	Out
120	DACK2-	ISA DMA 2 Acknowledge strobe.	Out
121	SD14	ISA System Data 14.	I/O
122	MASTER-	Not Supported.	In
123	SA04	ISA System Address 04.	Out
124	TC	ISA DMA Terminal Count.	In
125	SD15	ISA System Data 15.	I/O
126	SA03	ISA System Address 03.	Out
Key: In = TTL Input; Out = Output; OD = Open Drain/Collector Output; IS =Input with hysteresis			

Table 4. Pin Descriptions (5)

Pin	Pin Name	Description	Type
127	BALE	ISA Buffered Address Latch Enable.	Out
128	SA02	ISA System Address 02.	Out
129	SA01	ISA System Address 01.	Out
130	OSC	ISA 14.318 MHz utility clock. This clock is asynchronous to all other system clocks.	Out
131	SA00	ISA System Address 00.	Out
132	HISPEED	Input to select CPU speed. High=high speed.	In
133	SPKR	Speaker output, Open Collector, 24 mA drive.	OD
134	KDATA	Keyboard data.	I/O
135	KCLOCK	Keyboard clock.	I/O
136	PWRDN-	Low powers down peripheral circuits. Weak internal pull-up.	In
137	GND		
138	GND		
139	KBLOCK	Keyboard lock. Low blocks keyboard input.	In
140	SLCT	Parallel Port Printer is selected. Internal pull-up.	In
141	PE	Parallel Port Paper End. Weak internal pull-up.	In
142	BUSY	Parallel Port Printer Busy. Weak internal pull-up.	In
143	ACK-	Parallel Port Printer Acknowledge. Weak internal pull-up.	In
144	PD7	Parallel Port Data 7. Can sink 24 mA.	I/O
145	PD6	Parallel Port Data 6. Can sink 24 mA.	I/O
146	PD5	Parallel Port Data 5. Can sink 24 mA.	I/O
147	PD4	Parallel Port Data 4. Can sink 24 mA.	I/O
148	PD3	Parallel Port Data 3. Can sink 24 mA.	I/O
149	SLCTIN-	Parallel Port Select Printer.	OD 24
150	PD2	Parallel Port Data 2. Can sink 24 mA.	I/O
151	INIT-	Parallel Port Initialize Printer.	OD 24
152	PD1	Parallel Port Data 1. Can sink 24 mA.	I/O
153	ERR-	Parallel Port Printer Error. Internal pull-up.	In
Key: In = TTL Input; Out = Output; OD = Open Drain/Collector Output; IS = Input with hysteresis			

Table 4. Pin Descriptions (6)

Pin	Pin Name	Description	Type
154	GND		
155	PD0	Parallel Port Data 0. Can sink 24 mA.	I/O
156	AUTOFD	Parallel Port Printer Auto-Linefeed.	OD 24
157	STRB-	Parallel Port Data Valid Strobe.	OD 24
158	DCD2	Serial Port 2 Data Carrier Detect.	In
159	DSR2	Serial Port 2 Data Set Ready.	In
160	RXD2	Serial Port 2 Receive Data.	In
161	RTS2	Serial Port 2 Request To Send.	Out
162	TXD2	Serial Port 2 Transmit Data.	Out
163	CTS2	Serial Port 2 Clear To Send.	In
164	DTR2	Serial Port 2 Data Terminal Ready.	Out
165	RI2	Serial Port 2 Ring Indicator.	In
166	DCD1	Serial Port 1 Data Carrier Detect.	In
167	DSR1	Serial Port 1 Data Set Ready.	In
168	RXD1	Serial Port 1 Receive Data.	In
169	RTS1	Serial Port 1 Request To Send.	Out
170	TXD1	Serial Port 1 Transmit Data.	Out
171	CTS1	Serial Port 1 Clear To Send.	In
172	DTR1	Serial Port 1 Data Terminal Ready.	Out
173	RI1	Serial Port 1 Ring Indicator.	In
174	MA11	DRAM multiplexed memory address 11	Out
175	RAS3-	DRAM Row Address Strobe 3.	Out
176	RAS2-	DRAM Row Address Strobe 2.	Out
177	RAS1-	DRAM Row Address Strobe 1.	Out
178	RAS0-	DRAM Row Address Strobe 0.	Out
179	DP1	Not Supported.	I/O
180	DP0	Not Supported.	I/O
181	D15	DRAM Data Bit 15.	I/O
Key: In = TTL Input; Out = Output; OD = Open Drain/Collector Output; IS = Input with hysteresis			

Table 4. Pin Descriptions (7)

Pin	Pin Name	Description	Type
182	D07	DRAM Data Bit 7.	I/O
183	D14	DRAM Data Bit 14.	I/O
184	D06	DRAM Data Bit 6.	I/O
185	DRWE-	DRAM Memory Write Command.	Out
186	D13	DRAM Data Bit 13.	I/O
187	GND		
188	D05	DRAM Data Bit 5.	I/O
189	MA10	DRAM multiplexed memory address 10.	Out
190	MA09	DRAM multiplexed memory address 9.	Out
191	MA08	DRAM multiplexed memory address 8.	Out
192	D12	DRAM Data Bit 12.	I/O
193	D04	DRAM Data Bit 4.	I/O
194	MA07	DRAM multiplexed memory address 7.	Out
195	MA06	DRAM multiplexed memory address 6.	Out
196	D11	DRAM Data Bit 11.	I/O
197	D03	DRAM Data Bit 3.	I/O
198	MA05	DRAM multiplexed memory address 5.	Out
199	MA04	DRAM multiplexed memory address 4.	Out
200	D10	DRAM Data Bit 10.	I/O
201	D02	DRAM Data Bit 2.	I/O
202	MA03	DRAM multiplexed memory address 3.	Out
203	MA02	DRAM multiplexed memory address 2.	Out
204	D09	DRAM Data Bit 9.	I/O
205	VCC		
206	D01	DRAM Data Bit 1.	I/O
207	MA01	DRAM multiplexed memory address 1.	Out
208	MA00	DRAM multiplexed memory address 0.	Out
209	D08	DRAM Data Bit 8.	I/O
210	D00	DRAM Data Bit 0.	I/O
Key: In = TTL Input; Out = Output; OD = Open Drain/Collector Output; IS = Input with hysteresis			

Table 4. Pin Descriptions (8)

Pin	Pin Name	Description	Type
211	CASH3-	DRAM Column Address Strobe, High byte 3.	Out
212	CASL3-	DRAM Column Address Strobe, Low byte 3.	Out
213	CASH2-	DRAM Column Address Strobe, High byte 2.	Out
214	CASL2-	DRAM Column Address Strobe, Low byte 2.	Out
215	CASH1-	DRAM Column Address Strobe, High byte 1.	Out
216	CASL1-	DRAM Column Address Strobe, Low byte 1.	Out
217	CASH0-	DRAM Column Address Strobe, High byte 0.	Out
218	CASL0-	DRAM Column Address Strobe, Low byte 0.	Out
219	BDIS-	Boot source: Low = Internal Boot ROM; High = Internal Flash BIOS	In
220	XROMCS-	External ROM Chip Select; active low.	Out
221	LEDOUT-	IDE drive activity LED output; active low.	Out
222	GND		
223	HDRESET-	IDE Interface Reset output; active low.	Out
224	IDED07	IDE Data Bit 7.	I/O
225	HDD08	IDE Data Bit 8.	I/O
226	HDD06	IDE Data Bit 6.	I/O
227	HDD09	IDE Data Bit 9.	I/O
228	HDD05	IDE Data Bit 5.	I/O
229	HDD10	IDE Data Bit 10.	I/O
230	HDD04	IDE Data Bit 4.	I/O
231	HDD11	IDE Data Bit 11.	I/O
232	HDD03	IDE Data Bit 3.	I/O
233	HDD12	IDE Data Bit 12.	I/O
234	HDD02	IDE Data Bit 2.	I/O
235	HDD13	IDE Data Bit 13.	I/O
236	HDD01	IDE Data Bit 1.	I/O
237	HDD14	IDE Data Bit 14.	I/O
238	HDD00	IDE Data Bit 0.	I/O
239	HDD15	IDE Data Bit 15.	I/O
240	HDIOW-	IDE buffered I/O Write strobe.	Out
Key: In = TTL Input; Out = Output; OD = Open Drain/Collector Output; IS = Input with hysteresis			

Table 4. Pin Descriptions (9)

Memory and I/O Maps

MEMORY ADDRESS MAP

Table 5 shows the memory map for the “hardware level” OEMmodule 486.

	Address Range	Use	Block Size
Upper 63 MB Address Space	1000000h - 3FFFFFFh	Available for Memory	48 M
	0F00000h - 0FFFFFFh	Available for Memory	1 M
	0200000h - 0FEFFFFh	Available for Memory	13 M
	0100000h - 01FFFFFh	DRAM (Internal)	1 M
Lower 1 MB Address Space	00F0000h - 00FFFFFh	BIOS	64K
	00E8000h - 00EFFFFh	Flash Memory window (Reserved)	32K
	00E0000h - 00E7FFFh	ZF Reserved	32K
	00D0000h - 00DFFFFh	Empty	64K
	00C0000h - 00CFFFFh	Empty	64K
	00A0000h - 00BFFFFh	Empty	128K
	0000000h - 009FFFFh	DRAM (Internal*)	640K

Table 5. “Hardware Level” Memory Map

Table 6 shows the memory map for a “booted up” OEMmodule 486.

	Address Range	Use	Block Size
Upper 63 MB Address Space	1000000h - 3FFFFFFh	Available for Memory	48 M
	0F00000h - 0FFFFFFh	Available for Memory	1 M
	0200000h - 0FEFFFFh	Available for Memory	13 M
	0100000h - 01FFFFFh	DRAM (Internal*)	1 M
Lower 1 MB Address Space	00F0000h - 00FFFFFh	System BIOS	64K
	00E8000h - 00EFFFFh	Flash Memory window (Reserved)	32K
	00E0000h - 00E7FFFh	Reserved for extension ROM (empty)	32K
	00D0000h - 00DFFFFh	Reserved for extension ROM (empty)	64K
	00C8000h - 00CFFFFh	Reserved for extension ROM (empty)	32K
	00C0000h – 00C7FFFh	Video BIOS	32K
	00A0000h - 00BFFFFh	Empty	128K
	009F800h - 009FFFFh	Extended BIOS data	2K
	0000500h - 009F7FFh	Base DRAM (Internal)	639K
	0000400h – 00004FFh	System BIOS data	256
	0000000h - 00003FFh	Interrupt Vector table	1K

Table 6. “Booted Up” Memory Map

I/O ADDRESS MAP

Table 7 shows the I/O address map for the OEMmodule 486.

Address	Device
000h - 00Fh	DMA Controller 1 (8237 equiv.)
020h - 021h	Interrupt Controller 1 (8359 equiv.)
022h - 023h	System Control Port (Reserved)
040h - 043h	Programmable Timer (8254 equiv.)
060h, 062h - 064h	Keyboard Controller (8042 equiv.)
061h	Port B Status
070h - 071h	Real-Time Clock and NMI Mask
080h - 08Bh	DMA Page Registers (74LS61), 80h POST Code Output Port
092h	Fast A20 Gate and CPU Reset
0A0h - 0A1h	Interrupt Controller 2 (8359 equiv.)
0C0h - 0DFh	DMA Controller 2 (8237 equiv.) even addresses only
0EEh	Alternate A20 Gate Control
0EFh	Alternate CPU Reset Control
170h – 177h	EIDE Secondary Channel
1F0h - 1F7h	EIDE Primary Channel
2F8h - 2FFh	Serial 2
376h	EIDE Secondary Channel (HDCS1J)
378h - 37Fh	Parallel
3F6h	EIDE Primary Channel (HDCS1J)
3F0h - 3F7h	Floppy
3F8h - 3FFh	Serial 1

Table 7. I/O Map

Technical Note

Although the 80486 CPU can address 64K I/O addresses (16 bits), many I/O cards (those made for the ISA bus or the PC/104 bus) only decode the lower 10 address bits.

For example, a serial port at 3F8h actually appears at 3F8h, 7F8h, 0BF8h, 0FF8h, and so on. This is illustrated in Table 8, where the upper six bits of address are “don’t cares.”

Address	I/O Address Bits
03F8h	***0000 00***11 1111 1000
07F8h	***0000 01***11 1111 1000
0BF8h	***0000 10***11 1111 1000
0FF8h	***0000 11***11 1111 1000

Table 8. I/O Address Decode Limits

When designing I/O devices for embedded systems, avoid using addresses that might be in conflict with I/O devices that implement 10-bit decoding.

DRAM Interface

The OEMmodule 486 has 2 Mbytes of internal DRAM. This is enough DRAM for many embedded system applications, and, if so, no external DRAM is required.

The module also provides a DRAM interface with all the signals necessary for connecting standard EDO or fast page-mode 3.3 volt DRAMs.

Many DRAM configurations are supported, including standard 30-pin and 72-pin SIMM modules, ISO DIMM modules (single sided), and discrete components such as standard 1M x 4 and 4M x 4 DRAM chips. The interface is designed to support 70 nS or faster DRAMs.

The OEMmodule 486 can address up to 64M bytes of memory using 12 multiplexed address lines, MA0 – MA11 (16 Mbytes per bank) and four RAS/CAS strobe sets for implementing four separate banks of memory.

The DRAM interface consists of:

- Multiplexed Addresses MA00 – MA11
- Column Address Strobes CASL0- to CASL3- (low byte)
  CASH0- to CASH3- (high byte)
- Row Address Strobes RAS0- to RAS3-
- Bi-directional Data D0 – D15
- Memory Write Strobe DRWE-

DRAM interfaces provide a very high-speed data path to the CPU. To create a reliable DRAM memory subsystem, follow these guidelines:

- Keep leads between the module and DRAM devices as short as possible. Use a standard DRAM layout grid for discrete devices.
- Use 4-layer PCB technology, with power and ground planes.
- Power-bypass each discrete DRAM with .01 – .1 µF low-inductance capacitors. SIMM, DIMM, and SO memory modules have built-in power bypassing components. Bypass memory modules with low-inductance electrolytic capacitors. Keep capacitor leads as short as possible.
- Use 22-ohm series damping resistors on MA*nn*, CAS*n*-, RAS*n*-, and DRWE- signals between the module and the DRAM array. (You can use either discrete components or resistor packs.)

MEMORY BANK CONFIGURATIONS

The memory controller can support a number of different memory organizations. Memory is organized in up to 4 banks of up to 16 Mbytes per bank organized as 16-bit words. Each bank is supported by a RAS/CAS strobe set. CAS*n*L is assigned to the lower byte and CAS*n*H assigned to the upper byte in each bank.

- **Bank 0** RAS0-, CAS0L-, CAS0H- (Note that Bank 0 is occupied by the module's internal 2 Mbyte DRAM array.)
- **Bank 1** RAS1-, CAS1L-, CAS1H-
- **Bank 2** RAS2-, CAS2L-, CAS2H-
- **Bank 3** RAS3-, CAS3L-, CAS3H--

The BIOS interrogates the DRAM array and auto-configures the DRAM controller to accommodate the memory organization it finds. During its interrogation, it initially disables the 2 Mbyte internal DRAM array located in internal Bank 0 and if it finds memory in the external Bank 0, it leaves the internal Bank 0 disabled. If it finds no memory in an external Bank 0, it enables the internal Bank 0.

DRAM Example 1: Interfacing 72-Pin SIMM Modules

In this example, two 8 Mbyte 72pin SIMM DRAMs are interfaced. The design provides 16M bytes of DRAM. The DRAM in internal Bank 0 is disabled.

In this example:

- **U1** LS-byte and MS-byte of Bank 0 and Bank 1
- **U2** LS-byte and MS-byte of Bank 2 and Bank 3

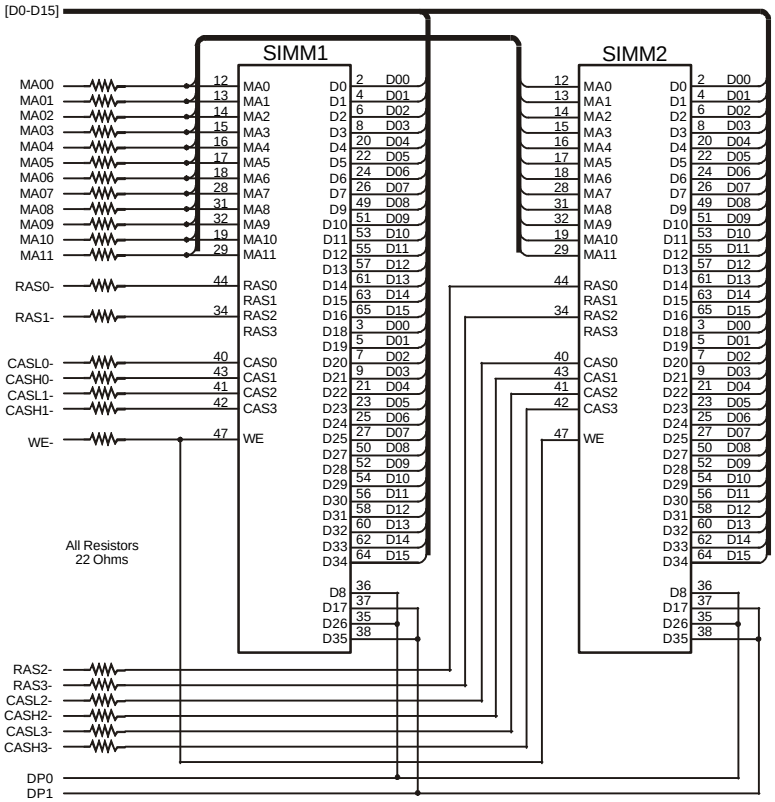


Figure 3. 72-Pin SIMM Example

DRAM Example 2: Interfacing Discrete DRAMs

In this example, four 1M x 4 discrete DRAMs are interfaced, providing an additional 2M bytes of memory for the OEMmodule 486. Bank 0 consists of the 2 Mbytes of DRAM in internal Bank 0. This design assigns 2 Mbytes of DRAM to Bank 1 for a total of 4 Mbytes for the system.

In this example:

- **U1 and U2** LS-byte of Bank 1
- **U3 and U4** MS-byte of Bank 1

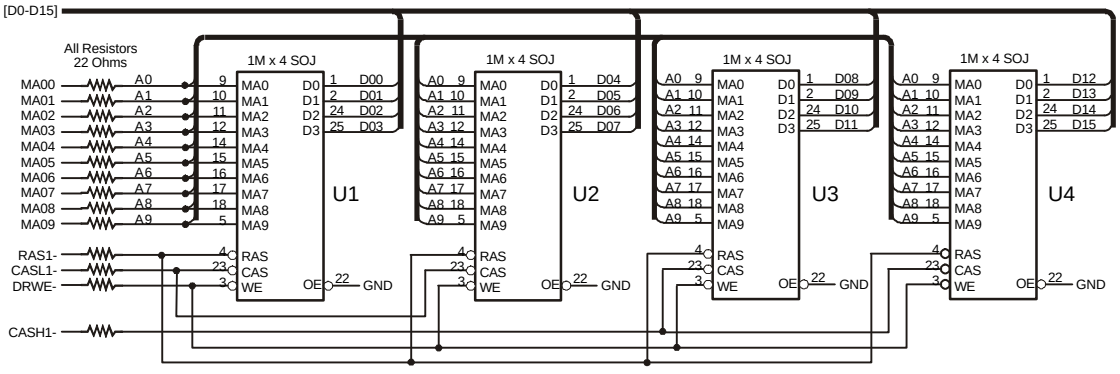


Figure 4. Discrete DRAM Example, 2M bytes

Memory Expansion Socket

The OEMmodule 486 supports an external memory expansion socket for adding an additional EPROM, Flash EPROM, or a non-volatile NOVRAM module to your system. This external socket can be used for up to one Mbyte of additional program memory that you can use for your application programs.

Example: Memory Expansion Socket

The following schematic shows how to attach a standard JEDEC byte-wide EPROM memory device to an OEMmodule 486 system. This circuit exemplifies the standard method of adding external byte-wide memory components to an OEMmodule 486-based system. In this example, the location of the memory device is determined by control signals CF0 - CF2.

Note the signal **XROMCS-**. This signal qualifies a byte-wide chip select for a 1 Mbyte region at F00000h – FFFFFFh. If this is the memory region you select for your memory expansion socket, no additional address decode logic is required.

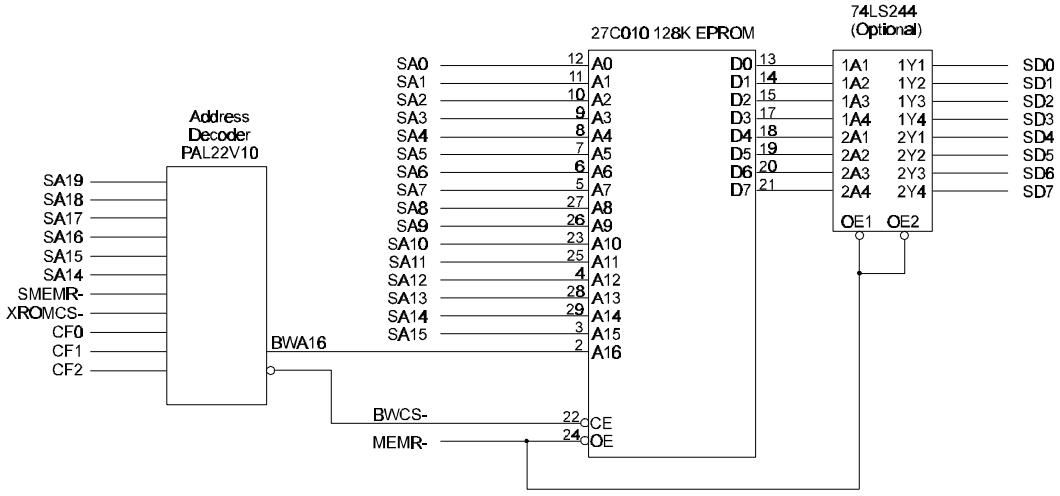


Figure 5. Memory Expansion Socket Example

The following is typical PAL code, written in ABLE, that could be used to program the address decode PAL shown in the example. It is written for a P22V10 PAL. It decodes SA19 – SA14 to provide a chip select signal for the expansion socket. CF0, CF1, and CF2 are jumper inputs that control the memory address location and size.

```
MODULE X_DECODE
TITLE 'EXTERNAL ROM DECODE'
XROM DEVICE 'P22V10'
"INPUTS:
 !XROMCS PIN 2;  "EXTERNAL ROM CHIP SELECT
 !SMEMR  PIN 3;  "MEMORY READ STROBE
 SA19    PIN 5;  "SYSTEM ADDRESS 19
 SA18    PIN 6;  "SYSTEM ADDRESS 18
 SA17    PIN 7;  "SYSTEM ADDRESS 17
 SA16    PIN 9;  "SYSTEM ADDRESS 16
```



```
 SA15    PIN 10;  "SYSTEM ADDRESS 15
 SA14    PIN 11;  "SYSTEM ADDRESS 14
 CF0     PIN 12;  "ADDRESS CONFIGURATION 0
 CF1     PIN 13;  "ADDRESS CONFIGURATION 1
 CF2     PIN 14;  "ADDRESS CONFIGURATION 2
"I/O:
 !BWCS   PIN 23;  "BYTE-WIDE CHIP SELECT
 BWA16   PIN 27;  "GATED SA16
 CADDR   PIN 25;  "C0000 ADDRESS (USED INTERNALLY)
 DADDR   PIN 26;  "D0000 ADDRESS (USED INTERNALLY)

" THIS CIRCUIT GENERATES CHIP SELECT AND MODIFIED SA16 FOR A 64K OR 128K BYTE
" MEMORY DEVICE AT CXXXXh - DXXXXh, OR AS SELECTED BY THE XROMCS- SIGNAL.
""
"  CF2..CF0  ADDRESS RANGE TABLE
" -------------------------------------
"  000       DISABLED (XROMCS ONLY)
"  001       16K AT DC000
"  010       32K AT D8000
"  011       64K AT D0000
"  100       80K AT CC000
"  101       96K AT C8000
"  110       112K AT C4000
"  111       128K AT C0000

EQUATIONS
BWCS.OE  = 1;  “OUTPUTS ARE ENABLED
BWA16.OE = 1;
CADDR.OE = 1;
DADDR.OE = 1;

CADDR = SMEMR & SA19 & SA18 & !SA17 & !SA16;
DADDR = SMEMR & SA19 & SA18 & !SA17 & SA16;
BWA16 = SA16 & !XROMCS;
BWCS = XROMCS
       # DADDR & CF2
       # DADDR & CF0 & SA15 & SA14
       # DADDR & CF1 & SA14
       # DADDR & CF1 & CF0
       # CADDR & CF2 & SA15 & SA14
       # CADDR & CF2 & CF0 & SA15
       # CADDR & CF2 & CF1 & SA14
       # CADDR & CF2 & CF1 & CF0;
END X_DECODE
```


Power Interface

The module's power interface consists of:

- VCC and Ground pins
- Powerfail monitor circuits

VCC AND GROUND PINS

For reliable operation, the OEMmodule 486 should be mounted on a multilayer printed circuit board that incorporates power and ground planes. Full-surface power and ground planes improve overall noise immunity. Generally, the power and ground planes are on two inner layers, with circuit traces on the top and bottom layers for easy accessibility. Internal power and ground planes also shield circuit traces, minimizing crosstalk interference.

For optimum reliability, connect all power and ground pins provided on the module to the power and ground planes. In addition, connect .1 µF and .001 µF low-inductance capacitors (surface-mount ceramic) in close proximity to each power pin, with short leads to VCC and Ground. Place at least one 33 µF low-voltage, low-inductance tantalum or aluminum miniature electrolytic nearby for power supply stabilization.

POWERFAIL MONITOR CIRCUITS

The OEMmodule 486 incorporates a voltage-level sensing circuit that monitors VCC. The circuit triggers a master reset if the supply voltage falls below a preset limit, 4.40V. The circuit guarantees a minimum 200 mS reset pulse width (guaranteed when VCC is above 1V), preventing erratic restarts if the power supply fluctuates.

A second circuit (optional) monitors an external voltage at PFI-, Pin 33. Internally, a comparator is set to 1.25V. When the voltage at PFI- falls below 1.25V, the OEMmodule 486 generates a PFO- signal, which you can use to reset circuits on your assembly. PFO- remains low until the PFI- signal goes above 1.25V. You can add external components to set the threshold level for this input. A typical circuit is shown in the following figure.

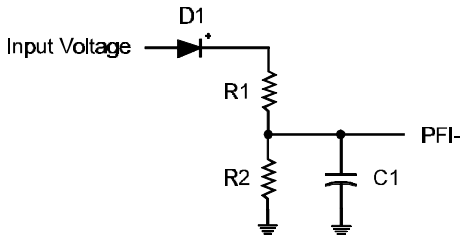


Figure 6. External Powerfail Voltage Input Circuit

Set the voltage level by adjusting the ratio of R1 and R2. C1 suppresses noise to prevent false triggering of the threshold detector.

The PFO- signal can be attached to MR-, Pin 35, to reset the system. Alternatively, it can be connected to IOCHCHK-, Pin 38, to generate an NMI. Using this approach, a voltage above 4.40V can be detected before system shutdown, allowing critical functions to be saved or protected (under control of the NMI interrupt handler). Another possibility is connecting PFO- to RTCIRQ-, Pin 36, a maskable interrupt normally used in conjunction with the Watchdog timer.

Note: Most interrupts are not shared resources. Do not directly connect more than one signal to an interrupt input. RTCIRQ-, however, is sharable between the real-time clock and an external input on the OEMmodule 486.

Note: If you connect PFO- to an interrupt, you must provide an appropriate interrupt handler in software to perform whatever function you want to occur when the power drops to the trigger point.

Serial Interface

The OEMmodule 486 provides two full-featured 16550-type asynchronous serial ports. The serial ports are treated as COM1 and COM2 devices by DOS. Table 9 lists the standard system resources that are allocated to the serial ports:

Serial Port	Typical Usage	I/O Address	Standard Interrupt
Serial 1	COM1	3F8–3FF	IRQ4
Serial 2	COM2	2F8–2FF	IRQ3

Table 9. Serial Port Resources

The I/O address and IRQ assignments for the serial ports are not configurable.

RS232C INTERFACE

The module's serial ports have a full complement of input and output handshaking lines. All serial port signals are at standard LSTTL levels. If you want RS232C compatibility, you must connect external devices.

RS232C signal levels are bipolar. A RS232C TRUE is $-3V \geq x \geq -12V$, and FALSE is $+3V \leq x \leq +12V$. There are a number of integrated circuits that can perform the TTL to RS232C level conversion. The following example shows a single-chip solution that has built-in voltage charge pumps to provide +9V and -9V signal levels from a standard +5V supply.

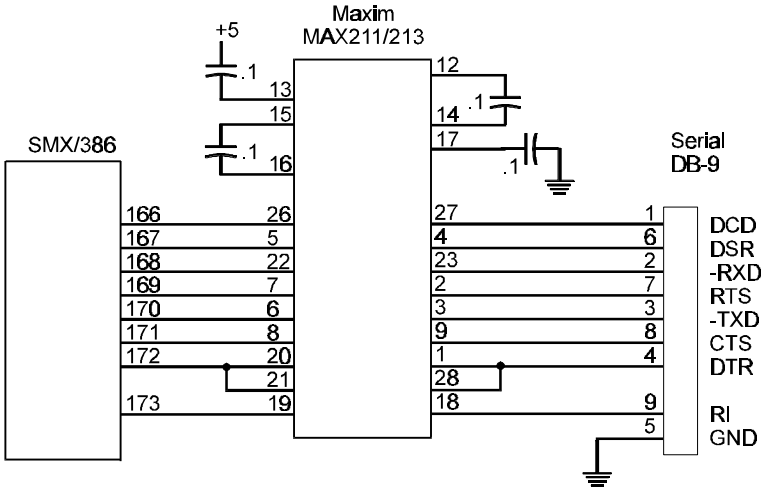


Figure 7. Typical TTL-RS232C Level Converter

Table 10 shows how serial ports, conditioned by RS232C level converters, can be wired to standard PC serial connectors. Two standards are shown, one for a DB9 connector and one for a DB25 connector.

Note: For the OEMmodule 486 serial ports to be compatible with standard PC serial peripherals you must provide RS232C level converters.

Serial 1 Pin	Serial 2 Pin	Signal	Function	In/Out	DB9	DB25
166	158	DCD	Data Carrier Detect	In	1	8
167	159	DSR	Data Set Ready	In	6	6
168	160	RXD	Receive Data	In	2	3
169	161	RTS	Request To Send	Out	7	4
170	162	TXD	Transmit Data	Out	3	2
171	163	CTS	Clear To Send	In	8	5
172	164	DTR	Data Terminal Ready	Out	4	20
173	165	RI	Ring Indicator	In	9	22
		GND	Signal Ground		5	7

Table 10. Serial Port Connections

CONSOLE REDIRECTION AND SOFTWARE DOWNLOAD

Beside the standard uses for the serial ports, the OEMmodule 486 provides serial services that are valuable to many embedded systems. These are *console redirection* and software *Manufacturing Mode*.

- Console redirection allows you to connect a serial terminal (or PC running a terminal emulation program) to act as the system host console.

- Manufacturing Mode lets you upgrade the contents of the Resident Flash Disk (RFD) over a serial port. Software is prepared on a host PC and then downloaded to the RFD.

Details about these features can be found starting on page **Error! Bookmark not defined.**.

INTERRUPT SHARING

The two serial port interrupt request lines comply with the interrupt sharing scheme described in the PC/104 Version 2.3 specification.

The interrupt request lines from Serial 1 and Serial 2 are buffered with open collector buffers and internally connected to inputs IRQ4 and IRQ3 respectively. An internal 1000 ohm termination resistor holds the signals at logic 0 until an interrupt occurs. Other interrupt sources can be wire-ORed with either of these IRQ lines as long as they also follow the PC/104 interrupt sharing convention. The interrupt request signals appear on module pins 117 (IRQ3) and 113 (IRQ4).

Note: A 1000 ohm pull-down resistor for each interrupt is provided in the module. Do not attach an external pull-down resistor.

The following circuit diagrams illustrate the two popular ways of implementing interrupt sharing. One is for sharing on the PC/104 bus, and the other is for sharing on the ISA bus.

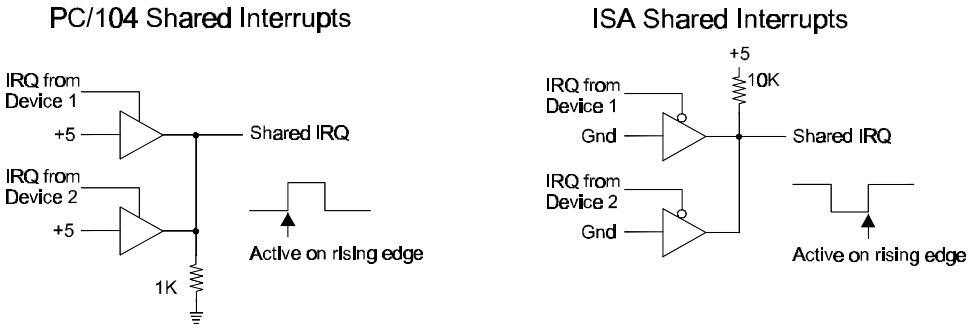


Figure 8. Typical Interrupt Sharing Circuits

Note that the interrupt-sharing methods for the PC/104 and ISA busses are not compatible. If you are designing a system with a mix of PC/104 and ISA peripheral cards, be careful to implement any shared interrupts you may have in your system with appropriate circuits. Also, appropriate logic must be implemented that provides the software interrupt handler to identify which particular device (maybe both) asserts the external IRQ. The logic is typically 1 bit of a device status register.

The PC/104 Scheme

In the PC/104 scheme, the interrupt request line from the peripheral is normally low and is asserted high to signal an interrupt. The interrupt request lines are disabled by the tri-state buffers when low and are held low by a 1K pull-down resistor. When an interrupt is asserted, the buffer is enabled, causing the IRQ to be pulled high by the buffer. It is then released and allowed to float low again, pulled down by the resistor.

The ISA Scheme

In the ISA scheme, when an expansion device is designed to share an interrupt with other devices, the interrupt request is normally high impedance, held high by a pull-up resistor, typically 10K ohms. When an interrupt is asserted, the signal goes low and is reset to high by the interrupt service routine. The interrupt is triggered by the low-to-high transition, just like the PC/104 scheme. Note, however, that the low to high transition is the leading edge of the interrupt signal in the PC/104 scheme and the trailing edge in the ISA bus scheme.

Parallel Interface

The OEMmodule 486 incorporates a full-featured multi-mode parallel port. In addition to the original IBM XT/AT output-only parallel port, it can also be configured as a PS/2 type bi-directional parallel port (SPP), or an Enhanced Parallel Port (EPP). The port can also be disabled if not used. When it is used, the parallel port requires the following PC resources (Table 11):

Typical Usage	I/O Address	Standard Interrupt
LPT1	378h - 37Fh	IRQ7

Table 11. Parallel Port Resources

The default interrupt for the parallel port is IRQ7. The parallel port's interrupt output signal appears on IRQ7OUT, Pin 99, adjacent to the IRQ7 input, Pin 98. If your application does not depend on the parallel port being interrupt driven, you can leave IRQ7OUT disconnected from IRQ7.

Parallel port control output signals are open collector and provide up to 24 mA drive current (active low). They generally are pulled up to +5 volts at the destination device.

Parallel port data I/O signals can provide up to 24 mA drive current (active low) and 12 mA (active high) when configured as output lines.

Table 12 and Table 13 summarize the parallel port register interface. In Table 12, "Base Address" indicates the port's base address, 378h.

Port Function	Address
Data Port	Base Address + 00h
Status Port	Base Address + 01h
Control Port	Base Address + 02h
EPP Address Port	Base Address + 03h
EPP Data Port 0	Base Address + 04h
EPP Data Port 1	Base Address + 05h
EPP Data Port 2	Base Address + 06h
EPP Data Port 3	Base Address + 07h

Table 12. Parallel Port Register Address Map

Port	D0	D1	D2	D3	D4	D5	D6	D7	Note
Data	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	1
Status	TMOUT (Note 1)	0	0	ERR-	SLCT	PE	ACK-	BUSY-	1
Control	STROBE	AUTOFD	INIT-	SLIN	IRQE	PCD	0	0	1
EPP Adr	AD0	AD1	AD2	AD3	AD4	AD5	AD6	AD7	2
EPP Data 0	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP Data 1	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP Data 2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP Data 3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2

Table 13. Parallel Port Register Bit Definitions

Note 1: These registers are available in all modes.

Note 2: These registers are only available in EPP mode.

Note 3: Bit definitions:

PDn	Parallel port data
TMOUT	10 µS time-out has occurred on the EPP bus. (This bit is only valid in EPP mode.)
ERR-	0 means an error has been detected.
SLCT	1 means that the printer is online.
PE	1 means that there is no paper in the printer.
ACK-	0 means that the printer has accepted a character and can now receive another.
BUSY-	0 means that the printer is busy. It is the complement of the level on the BUSY input.
STROBE	1 means there is valid data on the PDn bus. This bit is inverted and output onto the STROBE- pin.
AUTOFD	1 causes the printer to generate a linefeed after each line. This bit is inverted and output onto the AUTOFD- pin.
INIT-	0 causes printer to initialize.
SLIN	1 selects the printer. This bit is inverted and output onto the SLCT- pin.
IRQE	1 enables interrupts. An interrupt is generated on the positive-going ACK- input.
PCD	In bi-directional mode, 0 means output, 1 means input. Only valid in extended mode.

Table 14. Parallel Port Bit Definitions

Termination

In your motherboard design, provide 4.7K-ohm pull-ups (+5V) to the following parallel port outputs:

- STROBE-
- SLIN-
- INIT-
- AUTOFD-

Generally, if the parallel port will be connected to a cable for high speed data communication (as opposed to static digital output levels or static TTL level sensing), certain signals should have capacitors connected to ground. See the IEEE-1284 specification to determine the correct value of the capacitors.

Connect capacitors to the following signals and ground:

- PD0–PD7
- STROBE-

The following table shows the parallel port signals and includes the standard wiring of a DB25S connector, the standard connector used in PC systems for the parallel ports.

Pin	Signal	Function	In/Out	DB25 S Pin
155	PD0	Data bit 0	I/O	2
152	PD1	Data bit 1	I/O	3
150	PD2	Data bit 2	I/O	4
148	PD3	Data bit 3	I/O	5
147	PD4	Data bit 4	I/O	6
146	PD5	Data bit 5	I/O	7
145	PD6	Data bit 6	I/O	8
144	PD7	Data bit 7	I/O	9
140	SLCT	Printer selected	INPUT	13
141	PE	Out of paper	INPUT	12
142	BUSY	Printer busy	INPUT	11
143	ACK-	Character acknowledged	INPUT	10
149	SLIN-	Selects printer	OUTPUT	17
151	INIT-	Initialize printer	OUTPUT	16
153	ERR-	Printer error	INPUT	15
156	AUTOFD-	Auto feed	OUTPUT	14
157	STRB-	Output data strobe	OUTPUT	1
	GND	Signal Ground	N/A	18–25

Table 15. Parallel Port Connections

Floppy Interface

A PC-compatible floppy drive interface is supplied with the OEMmodule 486. In PC-compatible systems, the BIOS and DOS support two drives. These are configured using the BIOS Setup function. The floppy drive interface supports all standard PC floppy formats

Note: The OEMmodule 486 is equipped with a 1.8Mb internal Flash Disk that appears to DOS as a floppy disk drive. (It occupies a portion of the onboard Flash memory.) Use Setup to configure this to be the DOS A: or B: drive, or to disable it.

Table 16 lists the resources used by the floppy disk interface.

Resource	Function
I/O Address 3F0h-3F7h	3F2 FDC Digital Output Register (LDOR) 3F4 FDC Main Status Register 3F5 FDC Data Register 3F7 FDC Control Register (LDCR)
IRQ6	Interrupt
DRQ2 – DACK2	DMA Controller Channel

Table 16. Floppy Interface Resources

Capacity	Drive Size	Tracks	Data Rate
360K	5-1/4 inch	40	250 KHz
1.2M	5-1/4 inch	80	500 KHz
720K	3-1/2 inch	80	250 KHz
1.44M	3-1/2 inch	80	500 KHz

Table 17. Supported Floppy Formats

Select the types of drives connected to the floppy interface using the BIOS Setup function. The first drive appears to DOS as drive A:, and the second drive appears as B:.

Note: 1.2M drives can read floppy disks formatted for 360K bytes. 1.44M drives can read floppy disks formatted for 720K bytes.

Floppy Cable

Floppy drives are normally connected to a system using a ribbon cable. The pins on the OEMmodule 486 can be arranged for simple connection to a standard 34-pin ribbon cable connector. Use dual-row connectors with pins on .1 inch centers.

The typical PC connection for dual floppy drives uses a special cable with conductors 10 through 16 reversed (with a 180º twist) between the two floppy connectors. Using this arrangement, both floppy drives can be jumpered for Drive Select 1 (the “second” drive). The wires to drive A: have the twist.

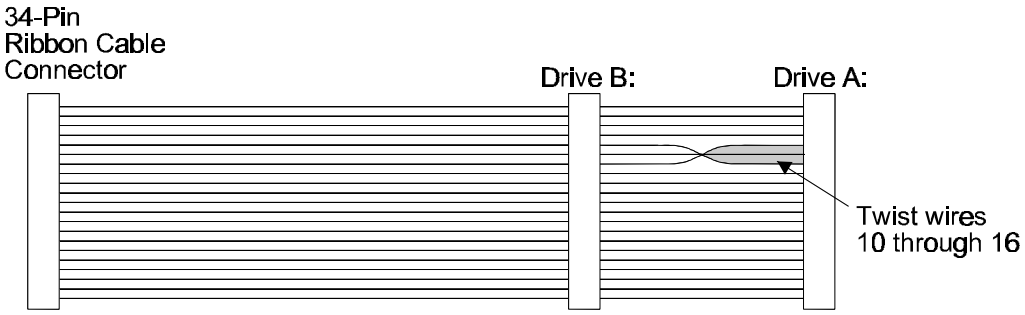


Figure 9. Typical Floppy Cable

Termination

Outputs to the floppy drive and from the floppy drive are 48 mA open collector. Pull-up resistors are required for proper termination.

Provide 330-ohm pull-ups for the following floppy interface signals:

- DSKCHG-
- WRPRT-
- INDEX-
- RDATA-
- TRK0-

Table 18 shows the pin connections for the floppy drive interface.

Module Pin	Floppy Pin	Signal Name	Function	In/Out
11	2	DENSEL	Speed/Precomp	
	4	N/A		N/A
	6	N/A	Key Pin	N/A
12	8	INDEX-	Index Pulse	In
13	10	MTR0-	Motor 0 On	Out
15	12	DRV1-	Drive 2 Select	Out
18	14	DRV0-	Drive 1 Select	Out
20	16	MTR1-	Motor 1 On	Out
22	18	DIR-	Direction Select	Out
23	20	STEP-	Step Pulse	Out
24	22	WDATA-	Write Data	Out
25	24	WGATE-	Write Gate	Out
26	26	TRK0-	Track 0	In
27	28	WRPRT-	Write Protect	In
28	30	RDATA-	Read Data	In
29	32	HDSEL-	Head Select	Out
30	34	DSKCHG-	Disk Change	In
	1–33	Ground	Ground	

Table 18. Floppy Drive Interface

IDE Drive Interface

The OEMmodule 486 is supplied with a standard IDE Hard Disk Interface. This is the standard interface used in PC-compatible systems for hard disk drives. Up to two drives can be connected. When two drives are installed, they are connected in a master-slave arrangement. The first hard disk drive (master) will appear as the C: drive to DOS. The second drive, if attached, will appear as D:. In Setup, the BIOS can be configured to autodetect most modern IDE hard disk drives.

The native IDE interface supports drives of up to 512M bytes each. Disk drive manufacturers often supply a utility program to support drives larger than this limit. Using these standard utilities, multi-gigabyte drives can be used with the OEMmodule 486.

IDE interface pins are arranged to allow easy attachment of a male PC-mounted ribbon-cable connector. The connector has two rows of pins on .1 inch centers. IDE drives can be attached to the drive interface with a 40-pin ribbon cable. Miniature drives sometimes require a cable adapter circuit board for translation between the standard .1 inch spacing connector and the smaller connector on the drive. Such adapters are generally supplied with the drive.

Table 20 lists the resources used for the IDE interface.

Resource	Function
I/O Address 1F0h-1F7h	Hard Disk Interface
3F6h	Digital output register/alternate status register
3F7h	Drive address
HDIRQ (IRQ14)	Interrupt

Table 20. IDE Interface Resources

Note: Methods of configuring IDE drives as *master* or *slave* vary from one manufacture to the next. It is not always possible to mix drives from different manufacturers. Review the technical specifications for your drives to make sure that they are compatible.

Termination

- Provide a 100-ohm series resistor in the HDRESET- signal line for noise immunity.
- Connect a 4.7K-ohm pull-up resistor (+5) to SLVACT.

Table 21 shows the pin connections for the IDE interface.

Pin	IDE Pin	Signal Name	Function	In/ Out	Pin	IDE Pin	Signal Name	Function	In/ Out
223	1	HDRESET-	Reset	Out		21	RSVD	Reserved	N/C
	2	GND	Ground			22	GND	Ground	
224	3	HDD07	Data Bit 7	I/O	240	23	HDIOW-	Write Strobe	Out
225	4	HDD08	Data Bit 8	I/O		24	GND	Ground	
226	5	HDD06	Data Bit 6	I/O	1	25	HDIOR-	Read Strobe	Out
227	6	HDD09	Data Bit 9	I/O		26	GND	Ground	
228	7	HDD05	Data Bit 5	I/O		27	RSVD	Reserved	N/C
229	8	HDD10	Data Bit 10	I/O	2	28	HDALE	Address Latch Enable	Out
230	9	HDD04	Data Bit 4	I/O		29	RSVD	Reserved	N/C
231	10	HDD11	Data Bit 11	I/O		30	GND	Ground	
232	11	HDD03	Data Bit 3	I/O	3	31	HDIRQ	Drive IRQ	In
233	12	HDD12	Data Bit 12	I/O	4, 58	32	IOCS16-	I/O Chip Select 16	In
234	13	HDD02	Data Bit 2	I/O	5	33	HDA1	IDE Address 1	Out
235	14	HDD13	Data Bit 13	I/O		34	RSVD	Reserved	N/C
236	15	HDD01	Data Bit 1	I/O	6	35	HDA0	IDE Address 1	Out
237	16	HDD14	Data Bit 14	I/O	7	36	HDA2	IDE Address 2	Out
238	17	HDD00	Data Bit 0	I/O	8	37	HDCS0-	IDE Chip Select 0	Out
239	18	HDD15	Data Bit 15	I/O	9	38	HDCS1-	IDE Chip Select 1	Out
	19	GND	Ground		10	39	LEDIN-		In
	20	KEY	Keyed Pin	N/C		40	GND	Ground	

Table 21. EIDE Drive Interface

NOTE: For maximum reliability, limit EIDE drive cables to less than 18 inches long.

Watchdog Timer

The watchdog timer triggers a reset or alarm if the application software fails to report it is running properly. A timer will alarm if not triggered by the application at least once every 1.6 seconds. If the watchdog timer does not receive the trigger when 1.6 seconds has elapsed, it generates the WDO- alarm signal on Pin 37. A BIOS Application Programming Interface (API) for the watchdog timer is implemented in the BIOS to simplify application development. Using the API, you can also monitor the BIOS and operating system.

You can use the watchdog timer alarm signal (WDO-) for any purpose in your design, but it's typically connected to one of three supervisory signals:

1. **MR-** This is the master reset input to the system. If WDO- is jumpered to this signal, the system will be reset and then restart when WDO- goes high.
2. **IOCHCHK-** This is an ISA failure signal that activates the Non Maskable Interrupt (NMI). The NMI occurs on the leading edge of WDO-.
3. **RTCIRQ**- This is the Real Time Clock Interrupt, IRQ8, and is often used for RTC alarm outputs. It is a maskable interrupt of lower priority than NMI. The interrupt would occur on the leading edge of WDO-.

You can also connect the output of the powerfail monitor to any one of these three control signals as well. The powerfail monitor output signal (PFO-) will go active (low) if power conditions violate the internal voltage thresholds. See the section "Power Interface" earlier in this chapter for details.

Note: Do not attempt to connect both PFO- and WDO- to the same interrupt signal.

The 1.6 seconds for the watchdog timer interval cannot be changed to other values.

Keyboard Port

The OEMmodule 486 keyboard port provides an interface to standard PC/AT or PS/2 keyboards. Table 22 shows the pins associated with the keyboard interface.

Module Pin	Signal Name	Function	5-Pin DIN
139	KBLOCK	Key Switch, disables keyboard	
134	KDATA	Keyboard Data	2
135	KCLOCK	Keyboard Clock	1
	GROUND	Ground return	4
	KEYBOARD POWER	Keyboard Power (+5 Vdc)	5

Table 22. Keyboard Connections

Keyboard Lock

The OEMmodule 486 also provides a standard PC keyboard lock mechanism. Shorting KBLOCK, Pin 139, to ground disables keyboard input.

Speaker Port

A standard PC speaker output signal appears at Pin 133. The pin supplies 24 mA of sink current to directly drive a small 8-ohm permanent-magnet speaker. Connect the speaker to the port using a circuit similar to the example shown in Figure 11. The 33 ohm resistor limits current through a low-impedance speaker coil.

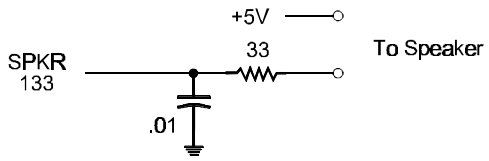


Figure 10. Typical Speaker Circuit

Real-Time Clock

The OEMmodule 486 incorporates a standard PC-compatible real-time clock. The real-time clock consists of a clock circuit with time, date, and alarm circuits, and CMOS RAM memory, used to retain system setup information in PC systems.

The real-time clock requires a 3.6 volt lithium cell to maintain the correct time and date values when power is off. Connect the battery to VBAT, Pin 31.

If the battery is not present when power is interrupted, the RTC will lose the current time and date, but the Setup configuration data will remain intact. This is because the CMOS RAM data is read from a Flash EPROM copy (inside the OEMmodule 486) at power up.

Note: If you will not be using a real-time clock battery in your application, leave VBAT, Pin 31, open.

Expansion Bus Interface

All the signals required to implement a PC/104 or ISA bus are brought out from the OEMmodule 486. To provide a PC/104 or ISA bus in your design, you add standard connectors and a few resistors.

The module can interface PC/104 expansion modules and/or ISA bus expansion boards as long as the total current drain on the bus signals does not exceed the PC/104 bus current specifications. The bus pinout of the module is arranged to provide for the simplest layout for either PC/104 bus headers or standard ISA edge card connectors.

Figure 12 and Figure 13 show examples of physical layouts for both PC/104 bus headers and ISA card-edge connectors.

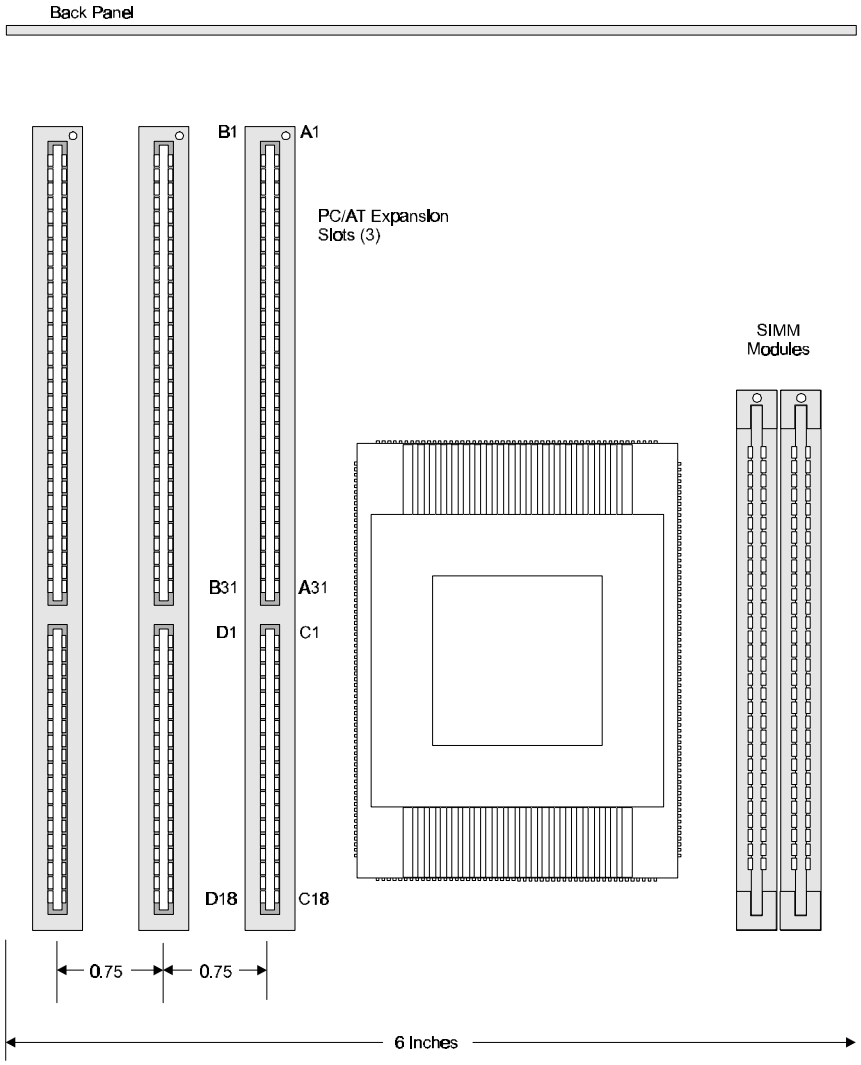


Figure 11. PC/AT Bus Example

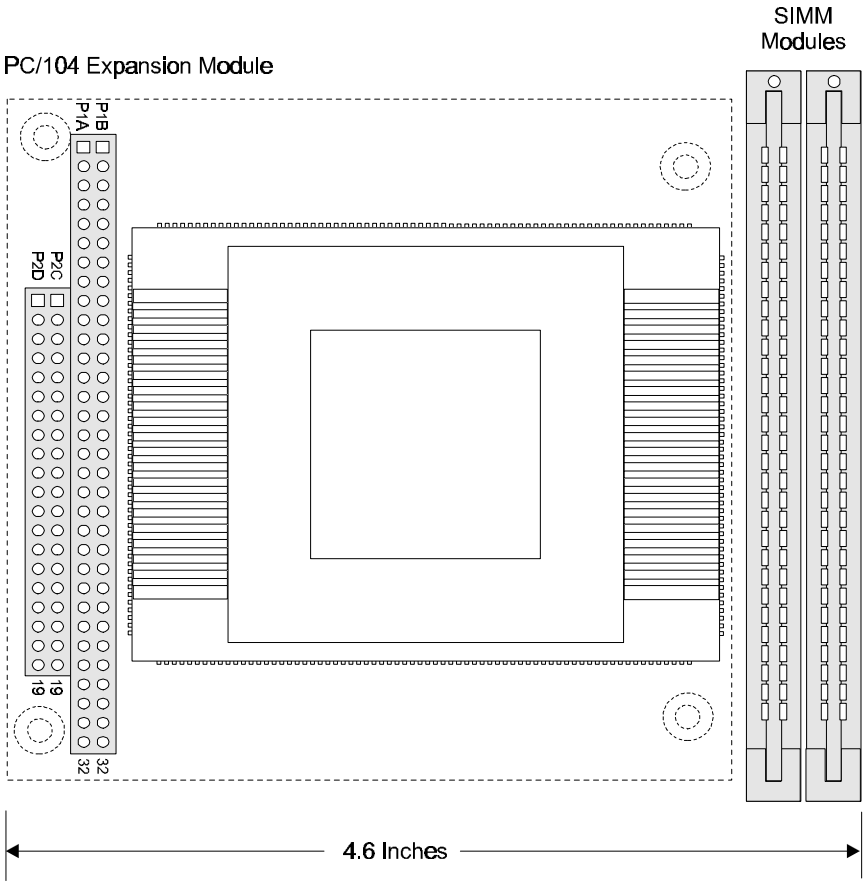


Figure 12. PC/104 Bus Example

Expansion Bus Interface

The following tables document the PC/104 expansion bus interface signals and corresponding standard ISA signals. The proper values for the external components are shown in the table.

Some expansion bus signals require external pull-up or pull-down resistors, while others are provided in the module. Resistors are left to be added externally for several reasons:

1. PC/104 and ISA busses require different values. You determine which values are required for your design.
2. When implementing a PC/104 or ISA bus, you may want to provide termination in the form of AC terminators (“snubbers”) for some bus signals. An AC terminator consists of a resistor and capacitor connected in series between the signal and ground. You must determine the right values for your design.
3. It is often better to position termination resistors or networks near a connector.

Pin	ISA	Signal Name	Function	In/out	Internal Pull-Ups	External Pull-Ups
38	A1	IOCHCK-	Bus NMI input	In	4.7K PU	
39	A2	SD7	System Data bit 7	I/O	PU	4.7K PU
41	A3	SD6	System Data bit 6	I/O	PU	4.7K PU
42	A4	SD5	System Data bit 5	I/O	PU	4.7K PU
44	A5	SD4	System Data bit 4	I/O	PU	4.7K PU
45	A6	SD3	System Data bit 3	I/O	PU	4.7K PU
48	A7	SD2	System Data bit 2	I/O	PU	4.7K PU
49	A8	SD1	System Data bit 1	I/O	PU	4.7K PU
51	A9	SD0	System Data bit 0	I/O	PU	4.7K PU
52	A10	IOCHRDY	Processor Ready Ctrl	In	4.7K PU	
55	A11	AEN	Address Enable	I/O	10K PU	
59	A12	SA19	Address bit 19	I/O	PU	10K PU
63	A13	SA18	Address bit 18	I/O	PU	10K PU
68	A14	SA17	Address bit 17	I/O	PU	10K PU
72	A15	SA16	Address bit 16	I/O	PU	10K PU
76	A16	SA15	Address bit 15	I/O	PU	10K PU
80	A17	SA14	Address bit 14	I/O	PU	10K PU
84	A18	SA13	Address bit 13	I/O	PU	10K PU
89	A19	SA12	Address bit 12	I/O	PU	10K PU
93	A20	SA11	Address bit 11	I/O	PU	10K PU
97	A21	SA10	Address bit 10	I/O	PU	10K PU
103	A22	SA9	Address bit 9	I/O	PU	10K PU
108	A23	SA8	Address bit 8	I/O	PU	10K PU
112	A24	SA7	Address bit 7	I/O	PU	10K PU
116	A25	SA6	Address bit 6	I/O	PU	10K PU
119	A26	SA5	Address bit 5	I/O	PU	10K PU
123	A27	SA4	Address bit 4	I/O	PU	10K PU
126	A28	SA3	Address bit 3	I/O	PU	10K PU
128	A29	SA2	Address bit 2	I/O	PU	10K PU
129	A30	SA1	Address bit 1	I/O	PU	10K PU
131	A31	SA0	Address bit 0	I/O	PU	10K PU
PU = Pull-Up; Unspecified PUs are ~10K ohms						

Table 23. Expansion Bus Connector, A1 - A31

Pin	ISA	Signal Name	Function	In/out	Internal Pull-Ups	External Pull-Ups
	B1	GND	Ground	N/A		
40	B2	RESETDRV	System reset signal	Out	10K PU	
	B3	+5V	+5 volt power	N/A		
43	B4	IRQ9	Interrupt request 9	In	PU	Note 1 (p.49)
	B5	-5V		N/A		
46	B6	DRQ2	DMA request 2	In	PD	
	B7	-12V		N/A		
50	B8	0WS- (1)	Zero wait state	In	330 PU	
	B9	+12V		N/A		
	B10					
56	B11	SMEMW-	Mem Write (lower 1MB)	I/O	10K PU	
60	B12	SMEMR-	Mem Read (lower 1MB)	I/O	10K PU	
64	B13	IOW-	I/O Write	I/O	1K PU	
69	B14	IOR-	I/O Read	I/O	1K PU	
73	B15	DACK3- (1)	DMA Acknowledge 3	Out	4.7K PU	Note 4 (p.51)
77	B16	DRQ3 (1)	DMA Request 3	In	PD	Note 4 (p.49)
81	B17	DACK1-	DMA Acknowledge 1	Out	2.2K PD	
86	B18	DRQ1	DMA Request 1	In	PD	
90	B19	REFRESH- (1)	Memory Refresh	I/O	330 PU	
94	B20	SYSCLK	System clock (8 MHz)	Out	33 SER	
98	B21	IRQ7	Interrupt Request 7	In	PU	Note 1 (p.49)
104	B22	IRQ6	Interrupt Request 6	In	PU	Note 1 (p.49)
109	B23	IRQ5	Interrupt Request 5	In	PU	Note 1 (p.49)
113	B24	IRQ4	Interrupt Request 4	In	1K PD	Note 1 (p.49)
117	B25	IRQ3	Interrupt Request 3	In	1K PD	Note 1 (p.49)
120	B26	DACK2-	DMA Acknowledge 2	Out	4.7K PU	
124	B27	TC	DMA Terminal Count	Out	4.7K PD	
127	B28	BALE	Address latch enable	Out	10K PU	
	B29	+5V	+5 volt power	N/A		
130	B30	OSC	14.318 MHz clock	Out	22 SER	
	B31	GND	Ground	N/A		
PU = Pull-Up, PD = Pull-Down, SER = Series; Unspecified PUs are ~10K ohms (1) These signals are not supported.						

Table 24. Expansion Bus Connector, B1 - B31

Pin	ISA	Signal name	Function	In/out	Internal Pull-Ups	External Pull-Ups
53	C1	SBHE-	Bus High Enable	I/O	4.7K PU	
57	C2	LA23	Address bit 23	I/O	PU	
61	C3	LA22	Address bit 22	I/O	PU	
65	C4	LA21	Address bit 21	I/O	PU	
70	C5	LA20	Address bit 20	I/O	PU	
74	C6	LA19	Address bit 19	I/O	PU	
78	C7	LA18	Address bit 18	I/O	PU	
82	C8	LA17	Address bit 17	I/O	PU	
87	C9	MEMR-	Memory Read	I/O	10K PU	
91	C10	MEMW-	Memory Write	I/O	10K PU	
95	C11	SD8	System Data bit 8	I/O	PU	4.7K PU
100	C12	SD9	System Data bit 9	I/O	PU	4.7K PU
106	C13	SD10	System Data bit 10	I/O	PU	4.7K PU
110	C14	SD11	System Data bit 11	I/O	PU	4.7K PU
114	C15	SD12	System Data bit 12	I/O	PU	4.7K PU
118	C16	SD13	System Data bit 13	I/O	PU	4.7K PU
121	C17	SD14	System Data bit 14	I/O	PU	4.7K PU
125	C18	SD15	System Data bit 15	I/O	PU	4.7K PU
PU = Pull-Up; Unspecified PUs are ~10K ohms						

Table 25. Expansion Bus Connector, C1 - C18

Pin	ISA	Signal Name	Function	In/out	Internal Pull-Ups	External Pull-Ups
54	D1	MEMCS16-	16-bit memory access	In	330 PU	
4, 58	D2	IOCS16-	16-bit I/O access	In	330 PU	
62	D3	IRQ10 (1)	Interrupt Request 10	In	PU	Note 3 (p.49)
66	D4	IRQ11 (1)	Interrupt Request 11	In	PU	Note 3 (p.49)
71	D5	IRQ12 (1)	Interrupt Request 12	In	PU	Note 3 (p.49)
75	D6	IRQ15 (1)	Interrupt Request 15	In	PU	Note 3 (p.49)
3, 79	D7	IRQ14	Interrupt Request 14	In	PU	Note 1 (p.49)
83	D8	DACK0- (1)	DMA Acknowledge 0	Out	4.7K PU	Note 4 (p.49)
88	D9	DRQ0 (1)	DMA Request 0	In	PD	Note 4 (p.49)
92	D10	DACK5- (1)	DMA Acknowledge 5	Out	2.2K PD	Note 4 (p.49)
96	D11	DRQ5 (1)	DMA Request 5	In	PD	Note 4 (p.49)
101	D12	DACK6- (1)	DMA Acknowledge 6	Out	4.7K PU	Note 4 (p.49)
107	D13	DRQ6 (1)	DMA Request 6	In	PD	Note 4 (p.49)
111	D14	DACK7- (1)	DMA Acknowledge 7	Out	2.2K PD	Note 4 (p.49)
115	D15	DRQ7 (1)	DMA Request 7	In	PD	Note 4 (p.49)
	D16	+5V	+5 volt power	N/A		
122	D17	MASTER- (1)	Bus master assert	In	330 PU	

BIOS Setup

The OEMmodule 486 internal system BIOS (Basic Input Output System) supports a standard Setup function to configure system parameters. The BIOS uses these parameters during system initialization to establish default conditions.

Setup parameters are stored in two places on the OEMmodule 486:

- The primary location for Setup parameters is in the CMOS RAM part of the real-time clock. This is the standard location for Setup parameters in PC/AT-compatible computers.
- A copy of the Setup parameters is saved in an internal Flash (non-volatile) memory device. Should the backup battery fail, or if it is not present in the system, the BIOS copies the parameters saved in the Flash device into the CMOS RAM during system initialization.
- The SETUP parameter sets in CMOS and Flash have associated checksum values. Should both checksums indicate that SETUP tables are corrupted, a set of factory defaults will be loaded. These factory defaults are hard-coded in the BIOS.

USING SETUP

There are several ways to modify the module's Setup parameters.

1. **Console:** You can enter Setup from the system's console and manually modify the parameters.
2. **Re-direction:** You can enter Setup from re-direction mode and manually modify the parameters.
3. **Floppy File:** You may load a file from a floppy disk. This is convenient for setting up modules in a production environment.
4. **Manufacturing Mode:** You may use Manufacturing Mode to download configuration information over COM1. This is convenient for field upgrades and for setting up modules in a production environment when no floppy is available.

Note: When you change Setup parameters, the new values (except for time and date) do not take effect until you recycle the power.

Updating from a Console

The system's console can be a standard PC video card, display, and keyboard, or it can be a serial terminal (or PC running a terminal emulator program) using re-direction mode.

Using a serial terminal for the system console is accomplished by *console redirection*. A specially-wired serial cable triggers console redirection. Details for constructing a console redirection cable are given on page 52.

To enter the Setup function using the system's console, press the <Del> key during POST. In console redirection mode, press CTRL-C instead of <DEL>. There will be a message displayed on the screen when <DEL> can be used.

Details about the Setup parameters you can change are given on page 51.

Updating from a Floppy File

If your system has a floppy disk drive, you can initialize Setup parameters using a floppy disk file. This is a fast and convenient way to initialize systems during production or in the field. Using a floppy disk file ensures that each system is initialized to a standard configuration, and prevents errors that could be introduced by configuring systems manually.

Refer to page 53 for instructions about how to create and use floppy Setup files.

Manufacturing Mode

You can also program setup parameters over a serial port using Manufacturing Mode. Manufacturing Mode requires a "host system," such as a central desktop PC on the production floor, or a laptop portable for field upgrades.

Manufacturing Mode is triggered by a specially-constructed serial cable. Information about the manufacturing mode serial cable, and how to use Manufacturing Mode to upgrade your system are given on page **Error! Bookmark not defined.**.

INITIAL SETUP SCREEN

To enter or change SETUP parameters, you must have a working system with a console. (You may use a serial terminal attached to COM1 for a console if you do not have a standard PC video adapter, keyboard, and display attached.) To enter the SETUP function using the system's console, press the <DEL> key during *Power On Self Test* (POST). To enter the SETUP function using the re-direction mode, press CTRL-C during POST. There will be a message displayed on the screen when <DEL> can be used.

> **Note:** When you change SETUP parameters, the new values (except for time and date values) do not take effect until the power is recycled.

At the initial display screen you can choose from a variety of choices. Press the keyboard spacebar or Pg Up/Pg Down to change options, and press Enter to select an item. Within variable fields you can use the arrow keys to move around. Choices at the initial screen include:

- **Basic CMOS Configuration**—Use this screen to set standard CMOS options. This item is described in greater detail later in this section.
- **Custom Configuration**—Use this screen to set additional CMOS options. This item is described in greater detail later in this section.
- **Format Integrated Flash Disk**—Formats the Resident Flash Disk (RFD)
- **Reset CMOS to last known values**
- **Reset CMOS to factory defaults**— Sets Drive A to floppy 0 (1.44MB), Drive B to Flash Disk, and Drive C to IDE 0 (IDE Type 2).
- **Write to CMOS and Exit**—Select this item after you're finished making setup changes and wish to store them.
- **Exit Without Changing CMOS**—Use this selection to abort any setup changes you've made and exit the configuration process.

Basic CMOS Configuration Options

The following options can be set on the Basic CMOS Configuration screen.

- **Drive A:** and **Drive B:**—Select the type of floppy or other drive you have connected for the A: and B: drives. Choices available include: 360KB, 720KB, 1.2MB, 1.44MB, 2.88MB, ROM disk, RAM disk, and Flash disk. If no drive is connected, select "Not Installed."
- **Hard Drive C:** and **Hard Drive D:**—Select an IDE drive type from the following list:

  Use drive type 1 if you want to enter specific values for your drive. To find out what values to enter, use the drive manufacturer's drive documentation.

  Use drive type 2 for Autodetect. Most newer drives will respond with their drive values when queried by the BIOS. A SanDisk is also set up as a type 2.

  – Use drive type 3 for LBA geometry.
  – Use drive type 4 for phoenix CHS geometry.
  – Use Not Installed for a solid state disk, such as DiskOnChip or no disk.
- **1st Boot Device, 2nd Boot Device, 3rd Boot Device, and 4th Boot Device**—These fields are used to select the order the system follows when attempting to boot. For example, the system first tries to boot from the "1st Boot Device" and if it can't then tries the "2nd Boot Device" and so on, until a boot drive is found. The following choices are supported:
  – >Drive A:, >Drive B:, >Drive C:, Boot from the drive identifier entered
  – >Debugger Boot to the Debugger screen

Custom CMOS Configuration Screen

The Custom Configuration screen provides the following options:

- **System Speed**—The system speed can be switched between 8MHz, 33MHz, 66MHz, or 100MHz.
- **Parallel Port**—LPT1 can be selected as a Standard (AT), Bi-Dir (PS/2), EPP, or Disabled. The IRQ can be set to IRQ7 or Disabled.
- **Serial Ports**—COM2 can be Enabled/Disabled. The IRQ can be selected between IRQ3, IRQ4, or Disabled.

Console Redirection

Console redirection can be used to access Setup when your system does not have a video adapter, video display, and keyboard attached. It can also be used to remotely access, control, or configure a system.

Console redirection can also be used as a substitute for a normal PC video and keyboard. Note, however, that all output to the screen must use DOS services. If your application writes directly to screen RAM, it will not display on a remote console.

Normally, a terminal emulator program, such as ProComm, is used to access the OEMmodule 486 system using console redirection.

To access the target system's Setup functions, for example, run a terminal emulator program on the host computer. Configure the terminal emulator to communicate via COM1 at:

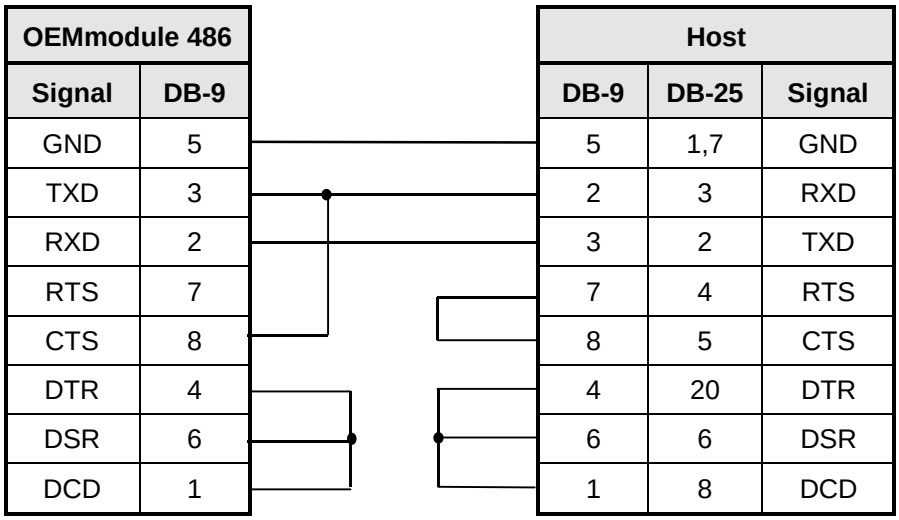
- 19,200 baud
- no parity
- eight data bits
- one stop bit

When you reboot the target system, the terminal emulator program will act as a serial console for the OEMmodule 486 system. You can enter Setup by pressing CTRL-C when prompted during POST.

CONSOLE REDIRECTION SERIAL CABLE

The OEMmodule 486 BIOS senses the COM1 port's cable wiring during system initialization following a power-on reset to automatically redirect console input and output.

Use the cable wiring shown in Figure 14 to connect a serial console to an OEMmodule 486 system.



OEMmodule 486		Host		
Signal	**DB-9**	**DB-9**	**DB-25**	**Signal**
GND	5	5	1,7	GND
TXD	3	2	3	RXD
RXD	2	3	2	TXD
RTS	7	7	4	RTS
CTS	8	8	5	CTS
DTR	4	4	20	DTR
DSR	6	6	6	DSR
DCD	1	1	8	DCD

Figure 13. Serial Cable for Console Redirection

Automatic CMOS Initialization

In a production environment, it is often desirable to automate the process of configuring your system's CMOS memory. By automating the process, you can improve productivity and eliminate errors that might be caused by manual setup.

The ZFUTIL utility allows you to write and read the CMOS settings. At this time, the write to file command is only available in the interactive mode. The read from file is available in the interactive and command line modes. See page 56 for more detailed information on the ZFUTIL.EXE utility.

Manufacturing Mode

The purpose of Manufacturing Mode is to reprogram the module's onboard Flash device remotely over a serial port. You can reprogram the system BIOS, video BIOS, CMOS configuration Flash backup, and application files independently.

The Manufacturing Mode feature is designed to be robust and does not require that the target module be able to boot. Of course, the module must have a functioning BIOS. You can update all of the software in a module's internal Flash device without any access to the module other than a connection to its COM1 serial

port. This permits simple setup processes during manufacturing and field updates using a notebook computer.

RECOVERING FROM ERRORS

Note that if an error (such as loss of power to the module) occurs while the Manufacturing Mode is reprogramming the onboard Flash device, it may be necessary to place the module in *Safe Mode* to be able to reboot it (by bringing module Pin 219, BDIS-, low). TNote that Manufacturing Mode only initiates reprogramming of the Flash after the entire file has been successful received and stored in the module's DRAM. Thus, errors during the transfer of a file from the PC to the module will not cause this failure and the Manufacturing Mode can simply be retried after the problem has been corrected.

MANUFACTURING MODE POST CODES

Manufacturing Mode issues POST codes while it is active. POST codes are hexadecimal values sent to I/O port 80h. You may build a POST code display into your system, or install a POST code plug-in board if you have an ISA bus slot available. A list of POST codes is provided in Appendix B (page 66).

MANUFACTURING MODE CABLE

Enable Manufacturing Mode by connecting a Manufacturing Mode cable to COM1 on the OEMmodule 486. The Manufacturing Mode function in the BIOS detects the Manufacturing Mode cable by sensing that the TXD signal is attached to the DCD signal.

Figure 15 illustrates the cable wiring needed to trigger Manufacturing Mode.

OEMmodule 486		Host		
Signal	**DB-9**	**DB-9**	**DB-25**	**Signal**
GND	5	5	1,7	GND
TXD	3	2	3	RXD
RXD	2	3	2	TxD
RTS	7	7	4	RTS
CTS	8	8	5	CTS
DTR	4	4	20	DTR
DSR	6	6	6	DSR
DCD	1	1	8	DCD

Figure 14. Manufacturing Mode Cable Wiring

Note: You must bring out the DCD signal on your OEMmodule 486 system's COM1 serial port to use the Manufacturing Mode feature.

Backup Fail Safe ROM

In addition to the system's BIOS, the module has a *Safe Mode* ROM(in a separate internal ROM), known as BDIS, that you can use to boot the system. You would use this feature if the BIOS fails, if the CMOS RAM is configured to put the module in a non-recoverable state, or when recovering from an interrupted or failed upgrade attempt of the module's BIOS.

The Safe Mode ROM has most of the same functions as the main BIOS. It can boot from a floppy disk, output to video, take keyboard inputs, and so forth. It is configured to boot from a single 1.44 Mbyte floppy drive. It does not have any user-settable configuration options as it does not use the module's CMOS configuration memory.

To boot your system using the Safe Mode ROM, connect a 1.44 Mbyte floppy drive as A:. Connect BDIS- (Pin 219) to ground. This enables the boot ROM and disables the BIOS.

Install a bootable floppy diskette in the floppy disk drive (A:) and apply power to your system. You may have a keyboard, VGA video adapter, and monitor attached.

Upgrading the BIOS

The module's ROM-BIOS resides in a Flash memory device which can be upgraded with a new BIOS image should the need arise. The following is an overview of the upgrade procedure. Release notes that accompany a BIOS upgrade give detailed instructions on how to upgrade your modules. The BIOS may be upgraded from a floppy disk or over a serial port using Manufacturing Mode. There are two utilities on the OEMmodule 486 BIOS upgrade diskette for use with the OEMmodule 486 and OEMmodule 486-based boards.

ZFUTIL.EXE

This program can be used when a floppy, IDE, or Compact flash device is available in your system. It supports two modes of operation: a) command line mode (default); and b) a menu driven mode to use if a keyboard and video device are present in the system. When you want to load the system or video BIOS, the utility defaults to ZF.ABS (system BIOS) or GENERIC.VBS (video BIOS). You can either rename the appropriate file to use these names or type in the full path and filename at the update prompt.

ZFHOST.EXE

This program must be used in conjunction with a manufacturing mode cable. The program is loaded on a host standalone PC connected to the target (OEMmodule 486-based board) via a manufacturing mode cable.

The functions that are present in this utility are:

Get Target Attention
Target System Information
Test Target Memory
Continue loading OS on target
Update System BIOS
Update Video BIOS
Update Flash from File (*)
Download Flash to File (*)
Erase Flash Block (*)
Read Target CMOS to File
Program Target CMOS from File
Download RFD Image from Target
Upload RFD Image to Target
Show Max Message Size
Exercise Link
Show Target Drives (*)
(*) Not available on this release.

BIOS INSTALL AND UPDATE PROCEDURES

There are two separate methods for installing or updating your system's firmware, depending on the resources available in your system.

Method A

If your system has a floppy, IDE, or Compact flash device, simply copy the files from the OEMmodule 486 BIOS Upgrade diskette to the drive you have available.Run the ZFUTIL program with the -i option, if you have akeyboard and monitor attached to your system. Use the arrow keys to navigate to the BIOS menu option and press enter to select the process to be performed from the menu. Run the ZFUTIL program in the line mode command, if you are in re-directin mode. When you want to load the system or video BIOS, the utility defaults to ZF.ABS (system BIOS) or GENERIC.VBS (video BIOS). You can either rename the file you wish to use to these names or type in the full path and filename at the update prompt.

Method B

If your system does not have a floppy, IDE, or Compact flash device, you can use the serial port to download the files. Two different circumstances must be considered:

1. **If yourflash BIOS is at Rev. B (12/11/98) or later.** Simply install the manufacturing mode cable (see page 54) on COM1 and run the ZFHOST program on the host computer using the arrow keys to select the menu item to upgrade the system.
2. **If your** flash BIOS is **pre-Rev. B or the fail-safe BIOS ROM (BDIS) jumper installed.** The pre-Rev. B BIOS and the BDIS BIOS do not support the ZFHOST program. To upgrade these BIOSs, you must install the BDIS jumper on the target system and follow the procedure detailed below.
   a) With both the host computer and the ZF target system off, connect a Manufactruing Mode cable between the target ZF system's COM1 serial port and the COM port you will use on the host computer. Specifications for a Manufacturing Mode cable are on page 54.
   b) Boot the host computer.
   c) Install the BIOS upgrade diskette in the host computer.
   d) Copy the image file with the video image required to the host computer's hard disk and rename the file **F-000000.**
   e) Start the host computer's terminal emulator. You can use any terminal emulator, such as ProComm, that supports **YMODEM Batch** protocol. Be sure the serial port you are using is configured for : 19.2K baud, No parity, 8 data bits, 1 stop bit.
   f) Power up the target ZF system. After a few seconds, it will begin to poll the host computer.
   g) On the host computer, initiate a **YMODEM Batch** transfer of the **F-000000** file you want to download.
   h) When the download is complete and the Flash device has been reprogrammed, power off both systems, remove the serial cable from the ZF system, remove the BDIS jumper, wait ten seconds, and then power it back on. Confirm that the new BIOS is working by observing the revision letter displayed during POST.

This completes the download upgrade procedure.

BIOS-Resident Debugger

The BIOS-resident debugger is only present in the revision B or early of the 486 BIOS. It is a powerful tool that you can use to experiment with your hardware and debug at a very low level. You can operate the debugger from the keyboard and video display, or over a serial port using console redirection.

The debugger includes:

- Basic display and change memory functions
- A disassembler
- Breakpoints
- Watchpoints
- Trace (single step)
- BIOS data display

CMOS MEMORY READ/WRITE ACCESS

Invoke the BIOS-resident debugger from the Initial Setup screen. The following information is displayed. (This is the debugger's breakpoint display.)

```
Type HELP for help, or G <Enter> to resume SETUP.

Embedded BIOS Debugger Breakpoint Trap
EAX = 0000000B  CS:EIP = F000:0000131A  EFL = 00000287  NG nz .. na .. PE .. CY
EBX = 00001F04  SS:ESP = 0000:00000FF6  EBP = 00000FDA  .. nt IOPL0 nv up EI ..
ECX = 00002000  DS:ESI = F000:00000653   FS = 4335       .. .. id vp vi al vm rf
EDX = 0000184F  ES:EDI = 9FC0:000011F1   GS = 0000
F000:0000131A   db     C3h               / “.” (195).

EB40DBG: _
```

Figure 15. Debugger Screen

DEBUGGER COMMAND LIST

Table 20 lists the debugger commands. Enter the command at the `EB40DBG:` prompt.

Command	Description
REBOOT	Cold boot the target
CONSOLE [CON¦COMn]	Set debug console
MASK x	Set debug mask for EDOSROM
WCOMx byte [n]	Write byte to COMx n times
MODE n	Set video mode
D[b¦w¦d] [addr]	Dump memory (bytes/words/dwords)
R[16¦32] [reg value]	Display registers
I[w¦d] port	Input from 8/16/32-bit I/O port
O[w¦d] port val	Output to 8/16/32-bit I/O port
U[16¦32] [addr]	Unassemble code
E addr byte […]	Enter bytes
V vector#	Display interrupt vector table pointer
T	Trace next instruction
+¦-	Inc/dec IP
G	Go (resume execution)
BP addr	Set breakpoint
BC bkpt#	Clear breakpoint
BL	List breakpoints
SO x	Route EDOSROM output to COMx
EA20¦DA20	Enable/disable A20 line
ECACHE¦DCACHE	Enable/disable cache
TORAM	Run BIOS from RAM
WP [addr]	Set/clear watchpoint
RC index	Read CMOS RAM data
WC index byte …	Write CMOS RAM data
RFL phys:phys len	Read nwords words from Flash
WFL phys:phys xxxx …	Write words to Flash
EFL phys:phys	Erase Flash block
LFL phys:phys	Lock Flash block
SFL phys:phys wdcnt value	Set Flash words to value
UFL phys:phys wdcnt addr	Update Flash from buffer

CSR index	Read data from chipset
CSW index data	Write data to chipset
RD¦WD unit sec hd trk addr	Read/write disk sector to/from buffer
BIOSDATA	Display BIOS data area
?¦HELP	Display debugger command help screen

Table 20. Debugger Commands

Layout Guidelines

The following are guidelines for laying out a circuit board to accommodate the OEMmodule 486.

PC Board

- Design for standard high-quality PCB stock.
- No special coatings or platings are required. Follow your manufacturer's recommendations.
- Design for four or more layers, with full power and ground planes on inner layers.
- Attach *all* module power and ground pins to their respective power and ground planes.
- As a minimum, provide power and ground planes under an external DRAM array (if you provide one in your design).

Power and ground planes reduce crosstalk on signal lines, provide for excellent power and ground distribution, and improve overall noise immunity. This is especially important if you are designing for a high-noise environment.

In addition, power and ground planes reduce RF emissions, making it easier to pass FCC emissions tests.

PCB Pad Layout

Figure 17 shows the pad dimensions and positions for optimum layout on a PC board.

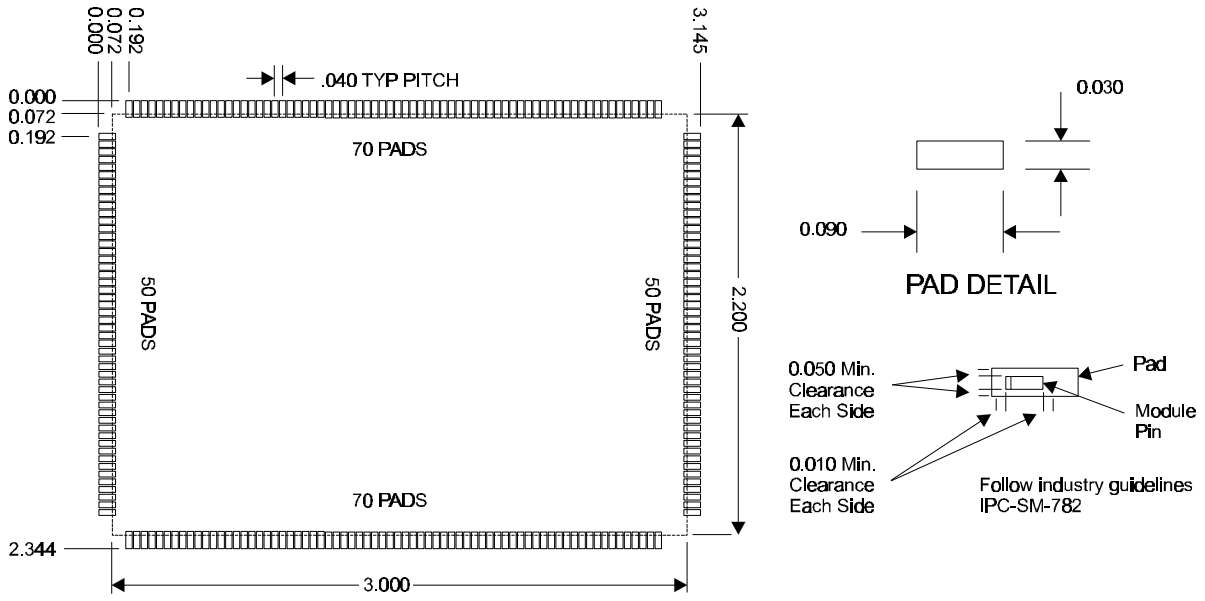


Figure 16. PCB Pad Layout

Follow industry guidelines as detailed in IPC-SM-782, "Surface Mount Design and Land Pattern Standard." This standard provides specifications for appropriate size, shape, and manufacturing tolerance of lands to ensure sufficient area for solder fillets. These lands provide optimum electrical connections and permit inspection and test.

Pad length: Pad must extend 0.010 in. (min.) beyond the end of the module pin, and 0.010 in. (min.) from the heel of the pin to the end of the pad on the inside.

Pad width: Pad must extend 0.005 in. (min.) beyond the module pin on both sides. Module pins are 0.014 in. wide on 0.040 in. centers.

Signal Groups

The wires for each supported function (memory, serial ports, parallel port, and so on) are grouped and ordered to optimize your PC board layout.

Figure 18 shows how pins are grouped and interleaved to minimize the number of vias and PC board layers required to connect signals to I/O connectors.

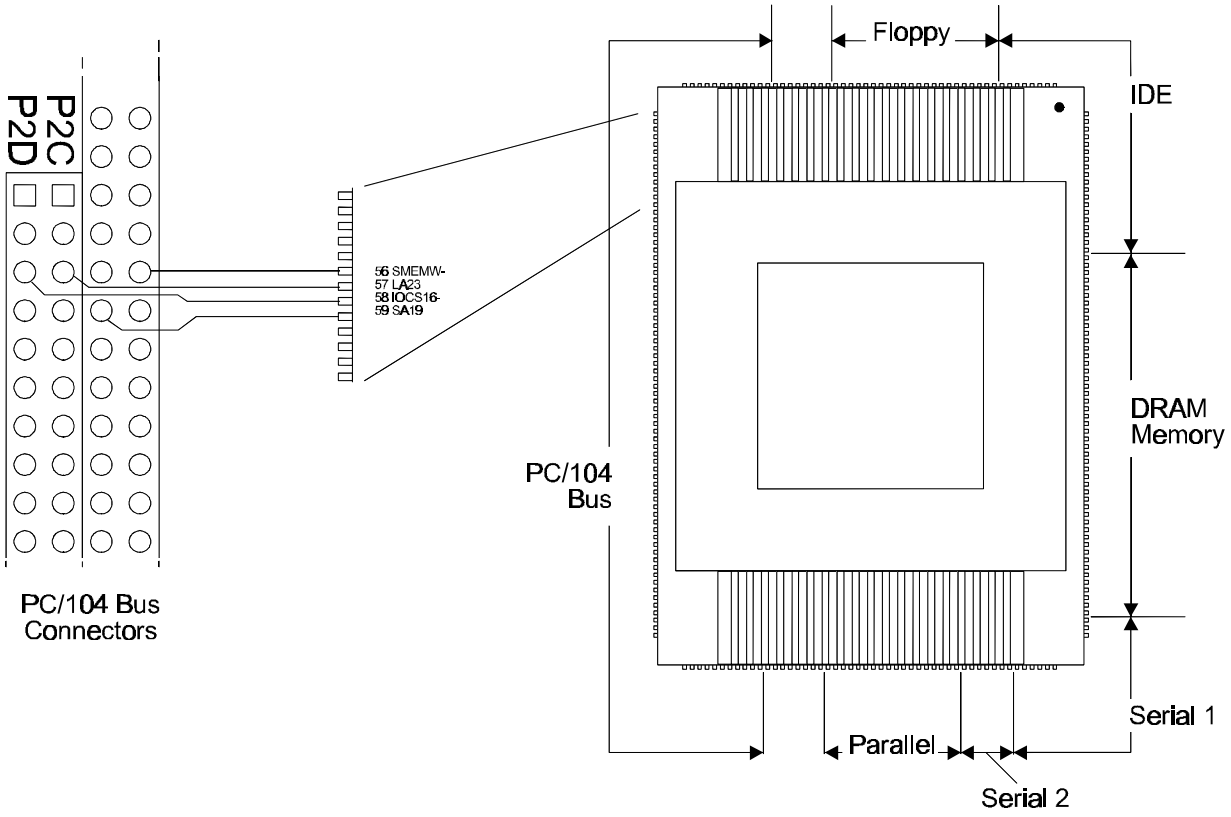


Figure 18. Signal Groups

No Components Under the Module

Do not mount components between the module and the circuit board. There are several reasons for this:

- Even though there is enough vertical clearance to mount small components under the module, the module's size and thermal mass can cause "thermal shadowing" which can make soldering quality in that region unpredictable.
- It is difficult to clean flux from under the module if components are mounted there.
- It is impossible to inspect and rework components mounted under the module.
- There is no minimum guaranteed clearance between the components mounted on the bottom of the module and the surface of the host printed circuit board. Future versions of the module could have less clearance in certain areas.

Circuit Design

Follow these recommendations for your circuit design to insure that your circuit is reliable and produces a minimum amount of electrical emissions.

- Provide a liberal number of power bypass capacitors. Use 0.1 µF and 0.01 µF low-inductance capacitors on integrated circuit power pins. Keep capacitor leads short to keep the inductance low.
- Provide one or more tantalum electrolytic capacitors on the board to stabilize the power plane.
- Condition input and output lines (serial, parallel, floppy, and so forth) to help reduce electrical emissions, especially if cables leave your enclosure. Roll off high-speed signal lines that go off the board with series inductors or ferrite beads, or bypass capacitors.
- During layout, run clock lines and other high speed lines first. This helps to keep these lines as short as possible. Minimize the number of vias on clock lines and other high-speed signal lines. Isolate any clock lines with grounded "guard traces" to minimize crosstalk distortion. If you have more than four layers in your PCB layout, run clocks on the layer closest to the power and ground planes.

The BDIS- Signal

The OEMmodule 486 incorporates a backup Fail-Safe ROM that can be used to boot the system should there be a problem booting with the main BIOS. This might occur, for example, if the BIOS was corrupted during reprogramming because of a power failure. The module can be placed in *Safe Mode* by bringing module Pin 219, BDIS-, low. ***Providing access to the BDIS- signal, through a jumper or via an unused pin of a connector, is highly recommended.***

Package Dimensions

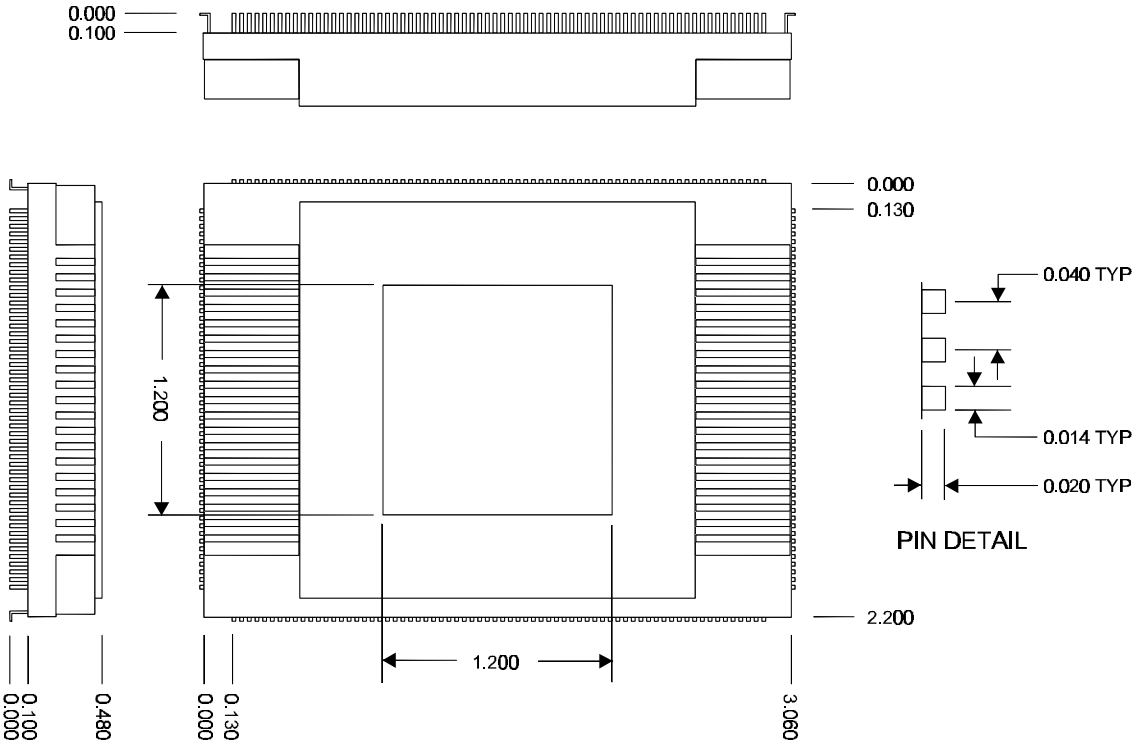


Figure 19. Package Dimensions

Package Dimension Notes:

1. Coplaniarity: 0.100 mm max.
2. Lead Position Tolerance: 0.200 mm max.
3. Recommended surface mount pad dimensions: 0.090 x 0.030 in.
4. Do not scale drawing.

Appendix A — Literature References

ISA System Architecture

MindShare, Inc., Tom Shanley and
Don Anderson
CompuServe: 72507,1054
Published by Addison Wesley, Inc.
http://www.mindshare.com/

AT Bus Design

Edward Solari
Annabooks
12145 Alta Carmel Ct., Suite 250
San Diego, CA 92128
http://www.annabooks.com/

Personal Computer Bus Standard P996
IEEE-1284 ECP Specification

Institute of Electrical and Electronic
Engineers, Inc.
445 Hoes Lane
Piscataway, NJ 08854
http://www.ieee.org

Technical data on the 486SX microprocessor:

Intel
1751 Fox Drive
Suite 29000
San Jose, CA 95131
http://www.intel.com/design/litcentr/litweb/intar.htm

Technical data on Maxim RS232C buffers:

Maxim Integrated Products, Inc.
510 N. Pastoria Avenue
Sunnyvale, CA 94086
http://www.questlink.com/index/maxim.html

The LIM 4.0 Expanded Memory Specification:

Lotus/Intel/Microsoft Expanded
Memory Specification, Version 4.0
Lotus Development Corporation
55 Cambridge Parkway
Cambridge, MA 02142

Appendix B — BIOS Post Codes

This list contains BIOS post codes and their meaning. POST codes are single-byte binary codes, expressed here as hexadecimal digits, that are output by the BIOS during the Power-On-Self-Test. The BIOS writes the codes to I/O port 80h.

These codes may be viewed on either a built-in POST code display (you can incorporate a display as a part of your system), on a POST code plug-in board, or even on a logic analyzer set to trigger on I/O writes to port 80h.

00h	POST beginning.
01h	CPU register test about to start.
02h	NMIs are disabled; delay starts.
03h	power-on delay finished.
04h	keyboard BAT done; reading keyboard SYS bit.
05h	disabling shadowing & cache.
06h	calculating ROM checksum, wait keyboard controller.
07h	checksum okay, keyboard controller free.
08h	verifying BAT command to keyboard controller.
09h	issuing keyboard controller command byte.
0ah	issuing keyboard controller data byte.
0bh	issuing pin 23,24 blocking & unblocking.
0ch	issuing keyboard controller NOP command.
0dh	testing CMOS RAM shutdown register.
0eh	checking CMOS checksum, updating DIAG byte.
0fh	initializing CMOS (if req'd every boot).
10h	initialize CMOS status register for date/time.
11h	disabling DMA, interrupt controllers.
12h	disabling Port B, disabling video display.
13h	initialize board, start auto-memory detect.
14h	starting timer tests.
15h	testing 8254 T2, for speaker, part B.
16h	testing 8254 T1, for refresh.
17h	testing 8254 T0, for 18.2Hz.
18h	starting memory refresh.
19h	testing memory refresh.
1ah	testing 15usec refresh ON/OFF time.
1bh	testing base 64KB memory.
1ch	testing data lines.
20h	testing address lines.
21h	testing parity (toggling).
22h	base 64KB memory read/write test.

Now we havememory, so we can use a stack to use Pcall, not Rcall

23h system initialization before vector table initialization.
24h initialize vector table.
25h reading 8042 for turbo switch setting.
26h initializing turbo data.
27h any initialization after vector table initialization is next.
28h setting monochrome mode.
29h setting color mode.
2ah toggle parity before optional video ROM test.
2bh initialize before video ROM check.
2ch control passed to video ROM.
2dh video ROM returned control.
2eh checking for EGA/VGA, adapter found.
2fh no EGA/VGA found, r/w test of video memory.
30h looking for video retrace signal.
31h retrace failed, checking alternate display.
32h alternate found, checking video retrace signal.
33h compare switches w/actual adapter type.
34h setting display mode.

Now we have a display. All code that putputs codes at 35h and above can use INT 10h to display messages.

35h check ROM BIOS data area at segment 40h.
36h setting cursor for power-on message.
37h displaying power-on message.
38h save cursor position.
39h display BIOS identification string.
3ah display "Hit <DEL> to ..." message.
40h preparing virtual mode test. verify from display memory.
41h preparing descriptor tables.
42h enter virtual mode for memory test.
43h enable interrupts for diagnostics mode.
44h initialize data for checking wraparound at 0:0.
45h checking for wrap, find total memory size.
46h write extended memory test patterns.
47h write conventional memory test patterns.
48h finding low memory size from patterns.
49h finding high memory size from patterns.
4ah check ROM BIOS data area again.
4bh check for <DEL>, clear low memory for soft reset.
4ch clearing external memory for soft reset.
4dh saving memory size.
4eh on cold boot, display 1st 64KB memory test.
4fh on cold boot, test all of low memory.
50h adjust memory size for 1K usage.
51h on cold boot, test high memory.
52h prepare for shutdown to real-mode.
53h saved registers & memory size, entering real-mode.
54h shutdown successful, restoring codepath.

55h disabling A20 line.
56h checking ROM BIOS data area again.
57h checking ROM BIOS data area some more.
58h clear the "Hit <DEL>" message.
59h test DMA page register.
60h verify from display memory (???).
61h test DMA0 base register.
62h test DMA1 base register.
63h checking ROM BIOS data area again.
64h checking ROM BIOS data area some more.
65h programming DMA controllers 0 & 1.
66h initializing INT controllers 0 & 1.
67h starting keyboard test.
80h issuing reset command & clearing output buffer.
81h check for stuck keys & issue test command.
82h initializing circular buffer.
83h check for locked keys.
84h check for memory size mismatch (CMOS/BIOSDATA).
85h check for password or bypass setup.
86h password checked. do programming before setup.
87h call the setup module.
88h back from setup, clear screen.
89h display power-on screen message.
8ah display "Wait..." message.
8bh do system & video BIOS shadowing.
8ch load standard setup parameters into BIOSDATA.
8dh check and initialize mouse.
8eh check floppy disks.
8fh configure floppy drives.
90h check hard disks.
91h configure IDE drives.
92h checking ROM BIOS data area again.
93h checking ROM BIOS data area some more.
94h setting base & external memory sizes.
95h memory size adjusted for 1K, verifying display memory.

Initialize any ROM BIOS extensions

96h initialization before calling C800h.
97h call ROM BIOS extension at C800h.
98h processing after extension returns.

Setup serial ports, parallel ports, NPX, keyboard, cache, wait states

99h configuring timer data area, printer base address.
9ah configuring serial port base addresses.
9bh initialization before coprocessor test.
9ch initializing the coprocessor.

9dh processing after coprocessor initialized.
9eh check external keyboard, kbdID, numlock settings.
9fh issue keyboard ID command next.
0a0h keyboard ID flag reset.
0a1h do cache memory test.
0a2h display any soft errors.
0a3h set keyboard typematic rate.
0a4h program memory wait states.
0a5h clear screen.
0a6h enable parity and NMIs.

Initialize ROM BASIC if available

0a7h initialization before calling E000h.
0a8h call ROM BIOS extension at E000h.
0a9h processing after extension returns.

Boot operating system

0b0h display system configuration box.
00h call INT 19h bootstrap loader.

Additional paths

0b1h test low memory exhaustively (optional).
0b2h test extended memory exhaustively (optional).

Download Mode issues POST codes while it is active. The following list describes the POST codes generated by Download.

0coh **Waiting for the serial interface to go quiet.** It implies that the PC is unexpectedly sending data to the module, or that the serial interface is too noisy. It is normal for this POST code to be displayed for one or two seconds as Download is starting, as Download is “listening” for random noise as part of its initial hardware tests.

0c1h **Waiting for, or receiving, a file header.** While waiting for a file header, Download sends upper case “C” characters to the PC. Since the file header has a maximum size of 1024 bytes, its transfer time should be too short to notice. If this POST code is being displayed and a file transfer is started at the PC, the POST code should change within two seconds (unless a hard disk or floppy has to “spin up” or network delays occur).

0c2h **Download completed.** Implies that a **Go** file, a **Reboot** file, or an escape character was sent to the module by the PC.

0c3h **Receiving a Go file.** Because the content of a **Go** file is irrelevant (it is the name of the file that matters), **Go** files are normally small (typically one byte), so this POST code should be displayed for less than two seconds.

0c4h Go file successfully received. Implies that Download has terminated and that the system is continuing to boot. This POST code should be overwritten by other (non-Download) POST codes within one second.

0c5h **Receiving a Reboot file.** Because the content of a **Reboot** file is irrelevant (it is the name of the file that matters), **Reboot** files are normally small (typically one byte), so this POST code should be displayed for less than two seconds.

0c6h **Receiving a Cmos file or reprogramming the module's CMOS or CMOS backup area in the onboard Flash device.** Typically this code is displayed for approximately three seconds, and should be displayed for no more than ten seconds.

0c7h **Analyzing the header of a Binary file or copying data from Flash to DRAM.** Some Flash chips can only be erased in multi-byte blocks (for example, blocks of 512 bytes or blocks of 64k bytes). If the area to be reprogrammed does not exactly match these block size restrictions, Download saves the current content of the block(s) in DRAM. This POST code should be displayed for less than one second.

0c8h **Receiving a Binary file.** Because binary files can be quite large, this POST code may be displayed for several minutes. PC software often displays progress data during a long download. While this POST code is being displayed, the PC's progress data should be changing. At 19.2k baud, it typically takes one or two minutes to transfer 64k of binary data from the PC.

0c9h **Erasing Flash blocks prior to reprogramming them with binary data.** This should take no more than one or two seconds per 64k of binary data from the PC.

0cah **Reprogramming Flash blocks with binary data.** This should take no more than two or three seconds per 64k of binary data from the PC.

0cdh **Unrecoverable error erasing the module's onboard Flash device.** This should not occur. Implies that either a power problem exists or that the module or its associated electronics are defective.

0ceh **Unrecoverable error writing to the module's onboard Flash device.** This should not occur. Implies that either a power problem exists or that the module or its associated electronics are defective.

0cfh **Invalid Binary file size or name.** Implies that the file sent from the PC was either improperly named or has improper content.

MANUAL REVISIONS

Revision	Date
OEMmodule 486 Release a	4/4/98
OEMmodule 486 Release d	2/3/99
OEMmodule 486 Release e	5/25/99

Manual Revision History

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